

# MS-7411

Ver:0B

## CPU:

AMD AM2+  
AMD AMD Athlon 64 X2  
AMD Athlon 64 FX  
AMD Athlon 64  
AMD Sempron CPUs

## System Chipset:

AMD - RS780M (North Bridge)  
AMD - SB700 (South Bridge)

## On Board Chipset:

BIOS - SPI  
Azalia CODEC - Realtek ALC888  
LPC Super I/O -- ITE IT8718F(GX)  
LAN - REALTEK 8111C  
IEEE1394 - JM381  
TMP - SLB9635TT1.2  
HWM W83201G

## Main Memory:

DDR II \* 4 (Max 4GB)

## Expansion Slots:

PCI Express X16 Slot \* 1  
PCI Express X1 Slot \* 3

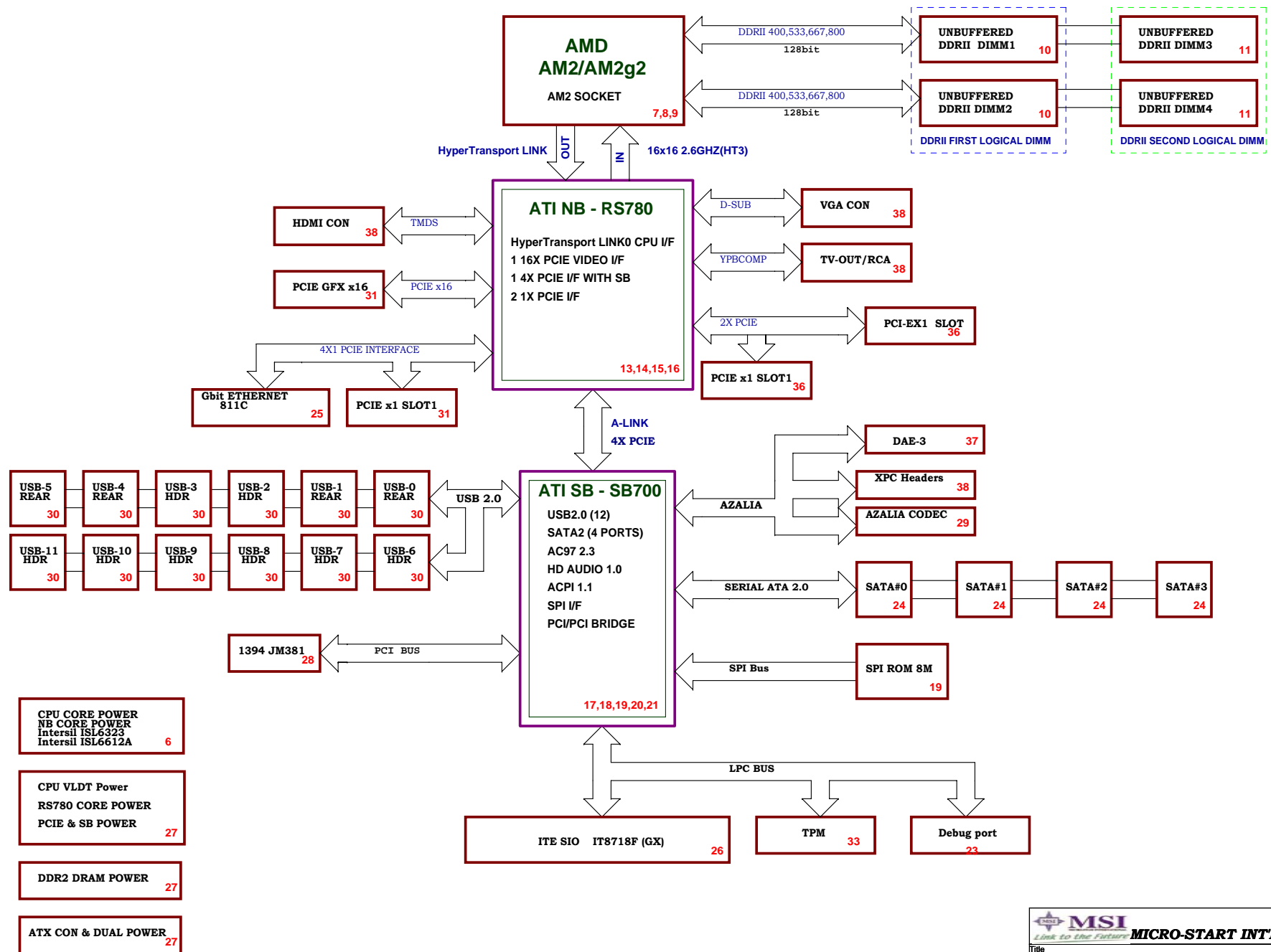
## Intersil PWM:

Controller - Intersil 6323 3 Phase

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# Project RS-780 BLOCK DIAGRAM





## SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTENTVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SMI#/EXTENTVNT1#		LPC_SMI#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#/GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

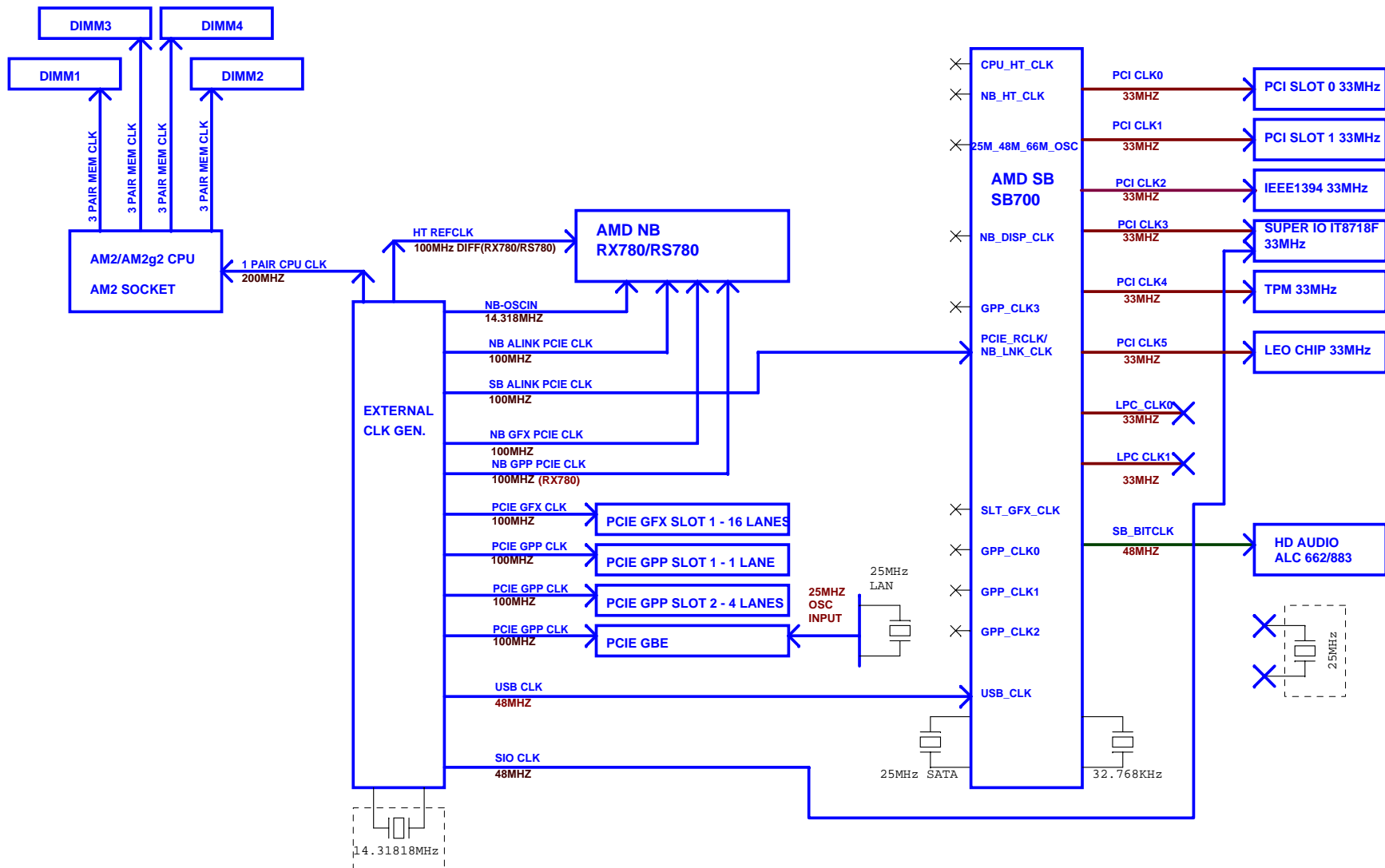
## Super I/O GPIO Config

GPIO Name	Type	Function Description	Pin	Page
VIDO5/GP27		LEO_GPIO2	20	26
VIDO4/GP26		LEO_GPIO1	21	26
VIDO1/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SMI#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	PREQ#0 PGNT#0	AD16	PCICLK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	PREQ#1 PGNT#1	AD17	PCICLK1
IEEE-1394	PCI_INTC#	PREQ#2 PGNT#2	AD18	PCICLK2

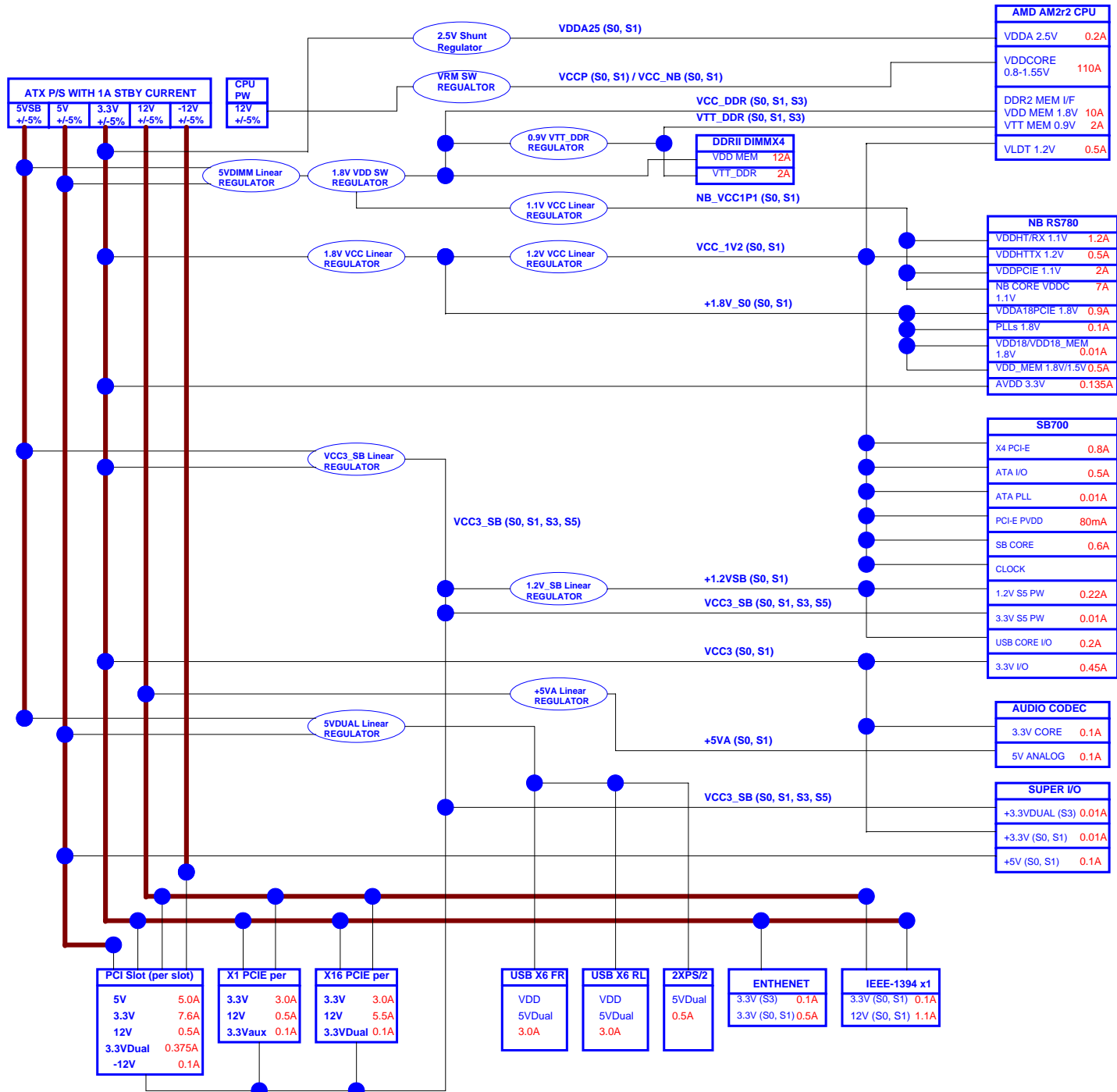




External clock mode  
Internal clock mode

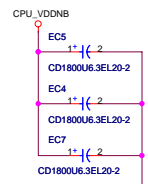
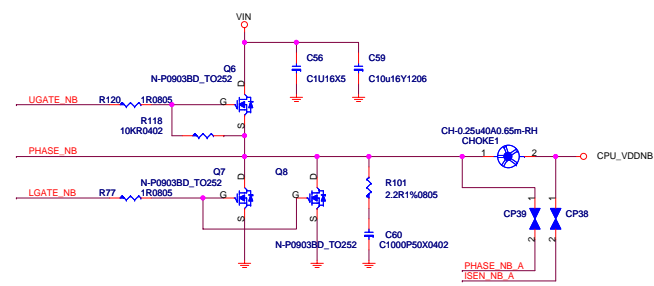
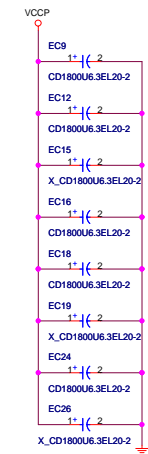
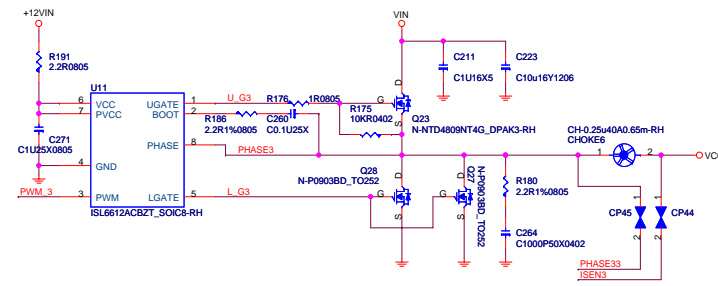
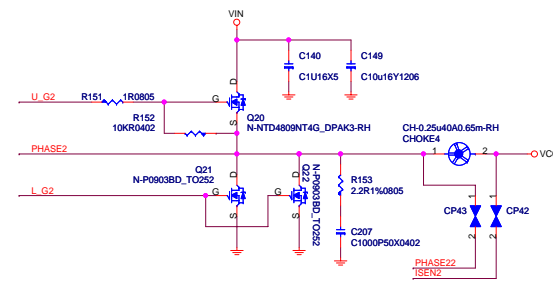
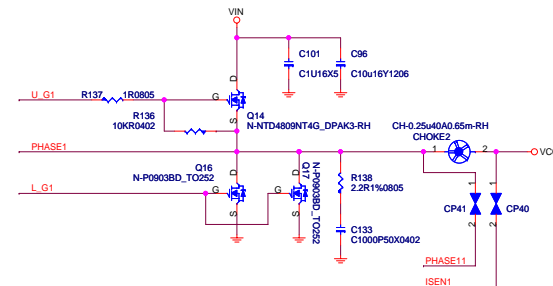
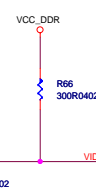
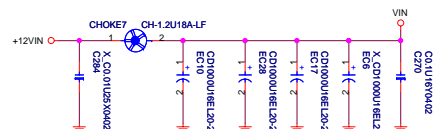
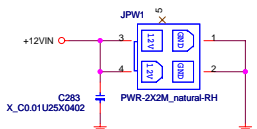
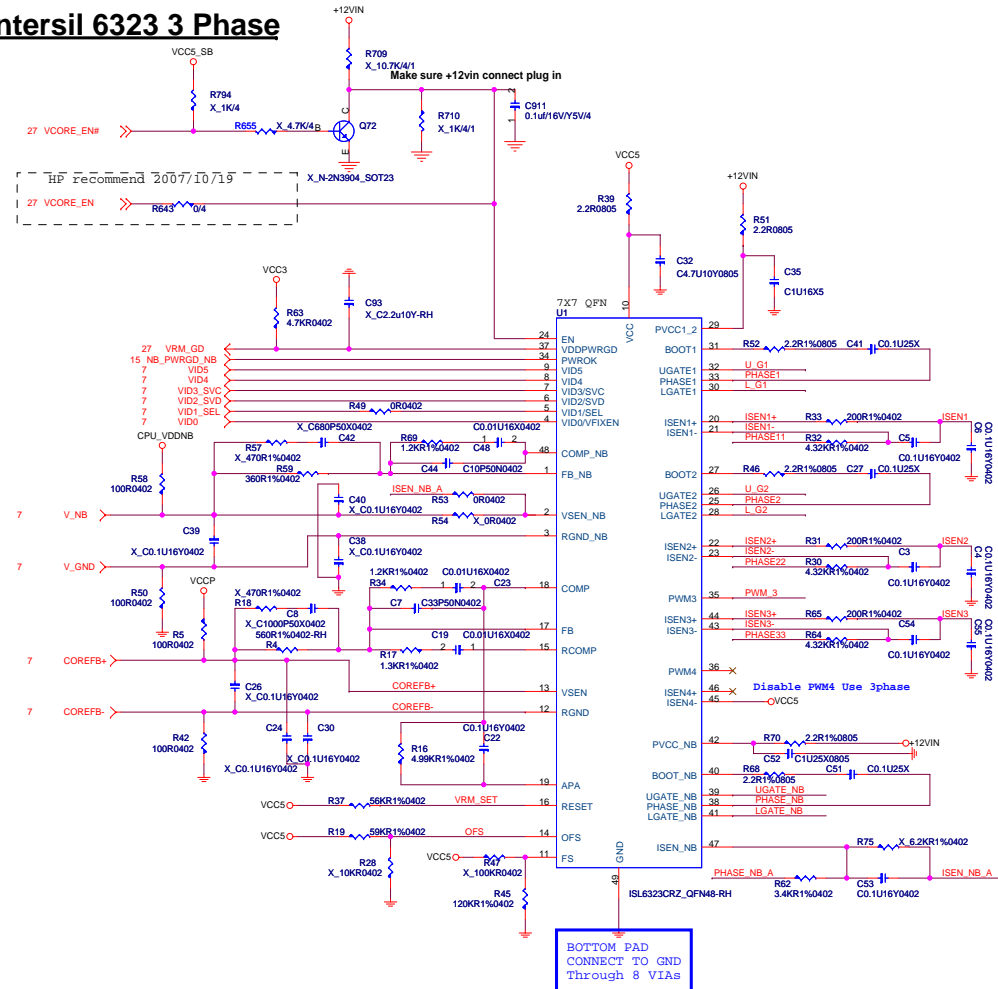


Power Deliver Chart





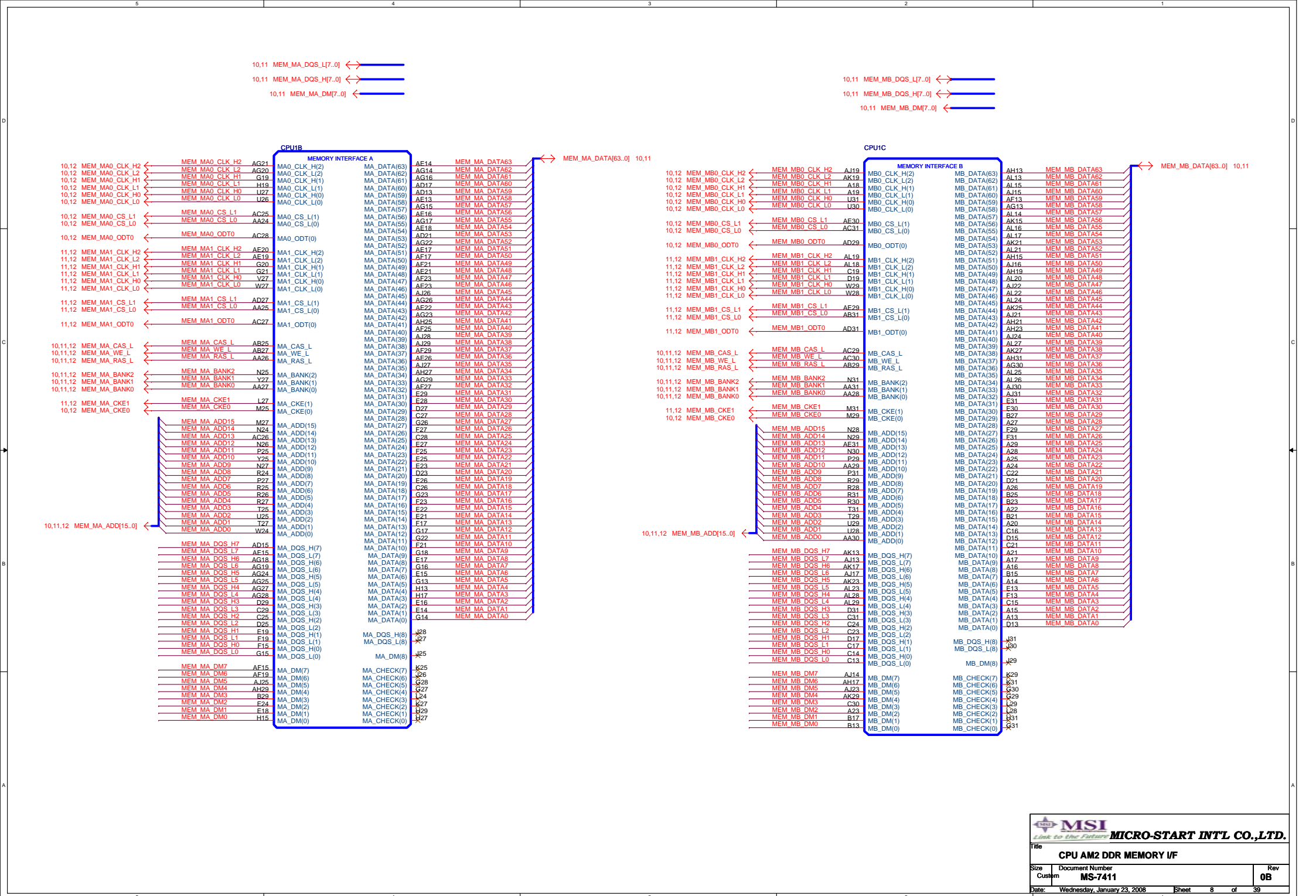
**Intersil 6323 3 Phase**





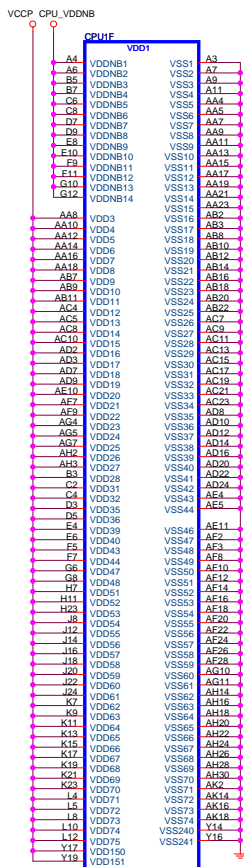




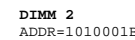
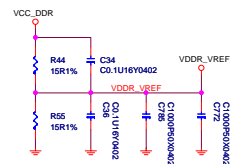
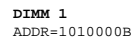




# CPU AM2 PWR & GND



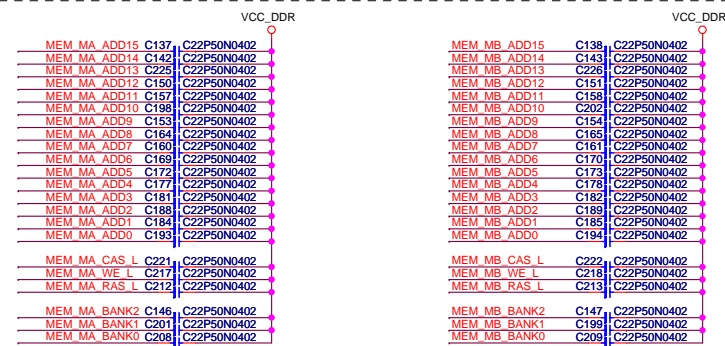
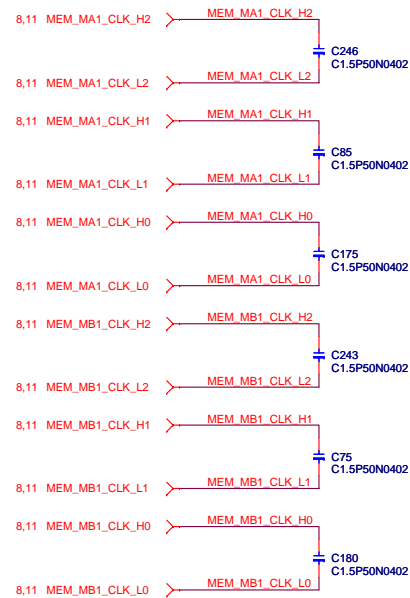
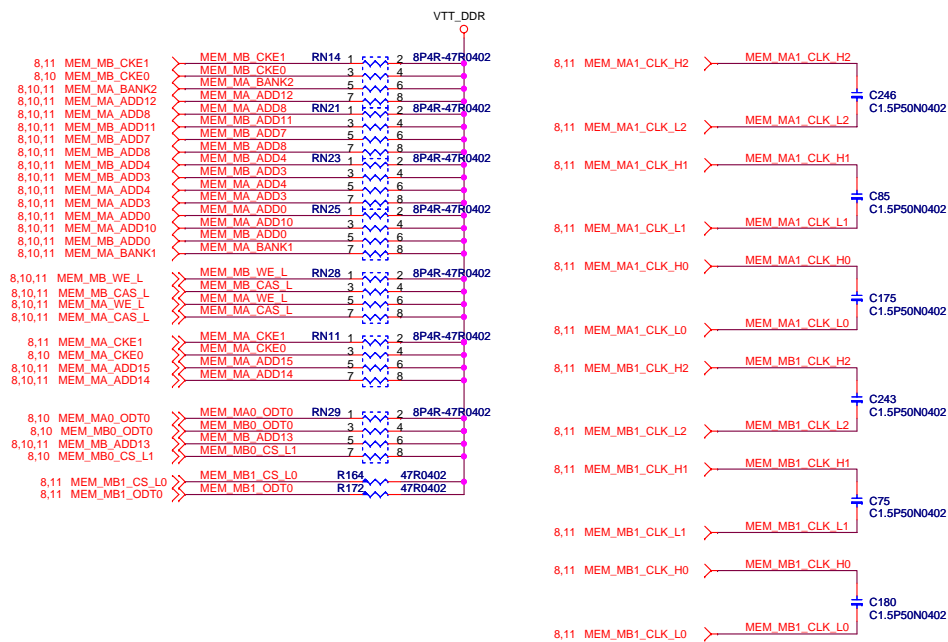
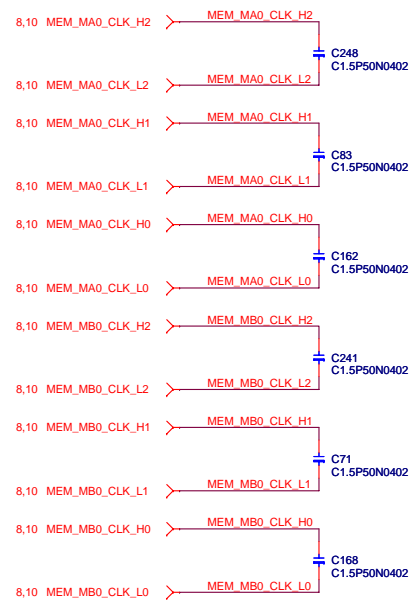
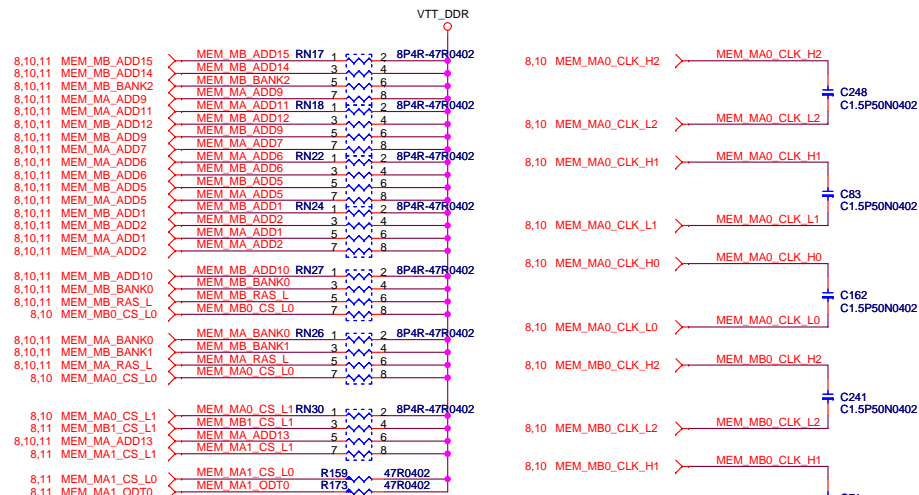






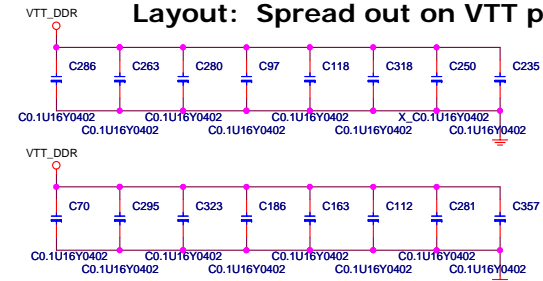




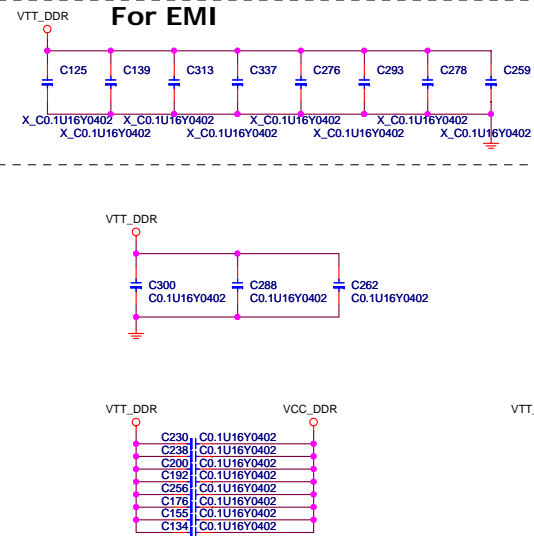


## Decoupling Between Processor and DIMMs

Layout: Spread out on VTT pour



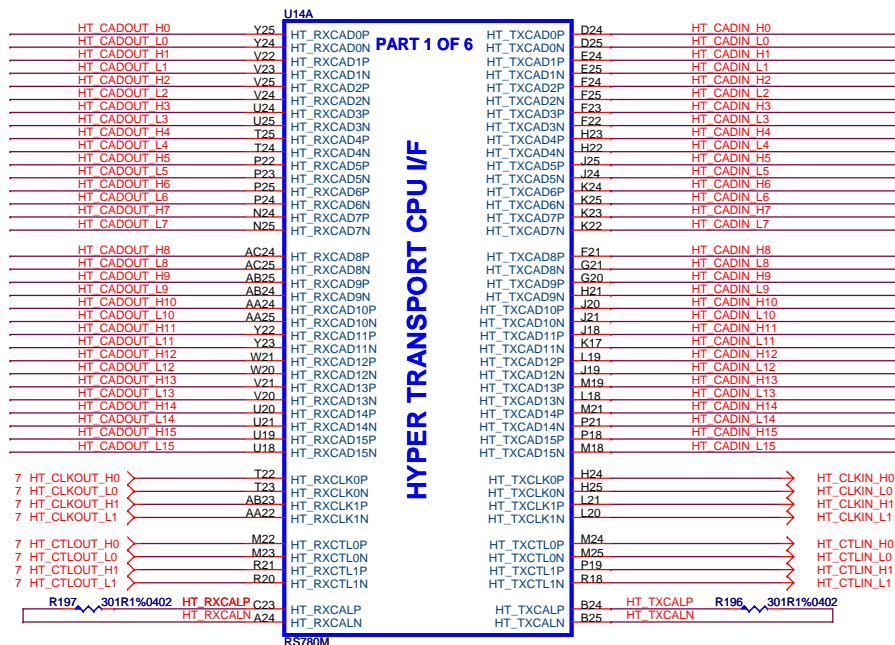
**For EMI**





# RS780-HT LINK I/F

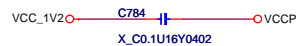
7 HT\_CADIN\_H[15..0] < HT\_CADIN\_H[15..0]  
 7 HT\_CADIN\_L[15..0] < HT\_CADIN\_L[15..0]  
 7 HT\_CADOUT\_H[15..0] > HT\_CADOUT\_H[15..0]  
 7 HT\_CADOUT\_L[15..0] > HT\_CADOUT\_L[15..0]



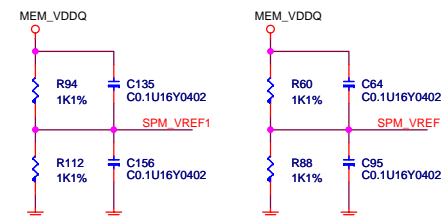
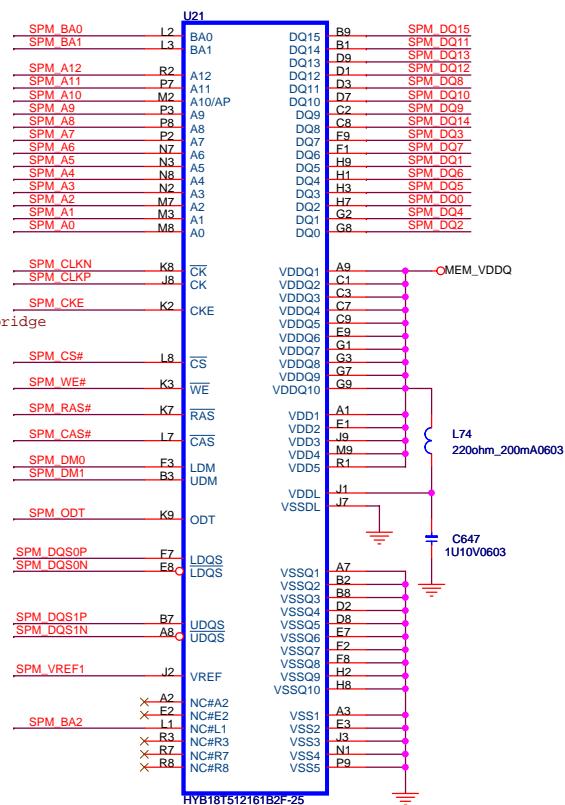
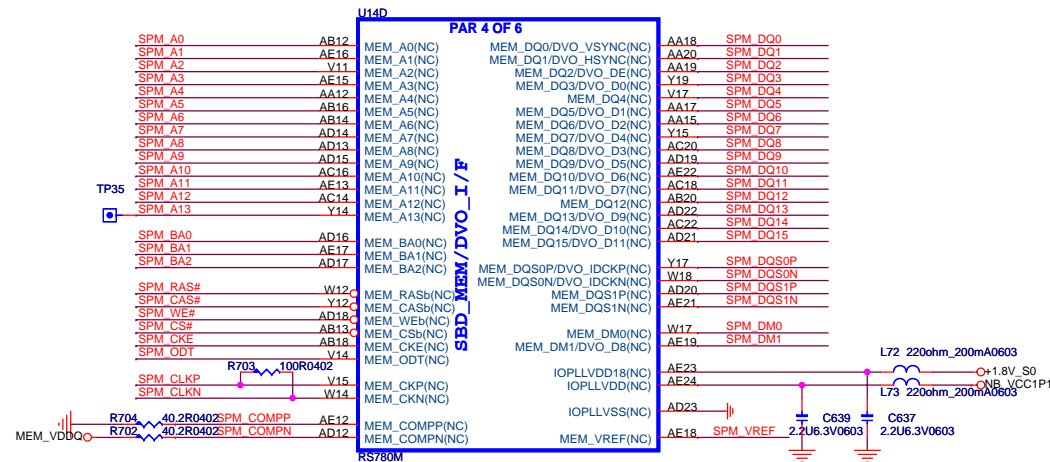
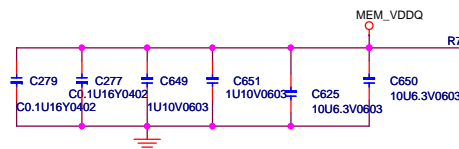
2:1 minimum space:height ratio.  
 Place resistor(s) within 1.0" of Northbridge balls.

2:1 minimum space:height ratio.  
 Place resistor(s) within 1.0" of Northbridge balls.

Decoupling Cap for HT.

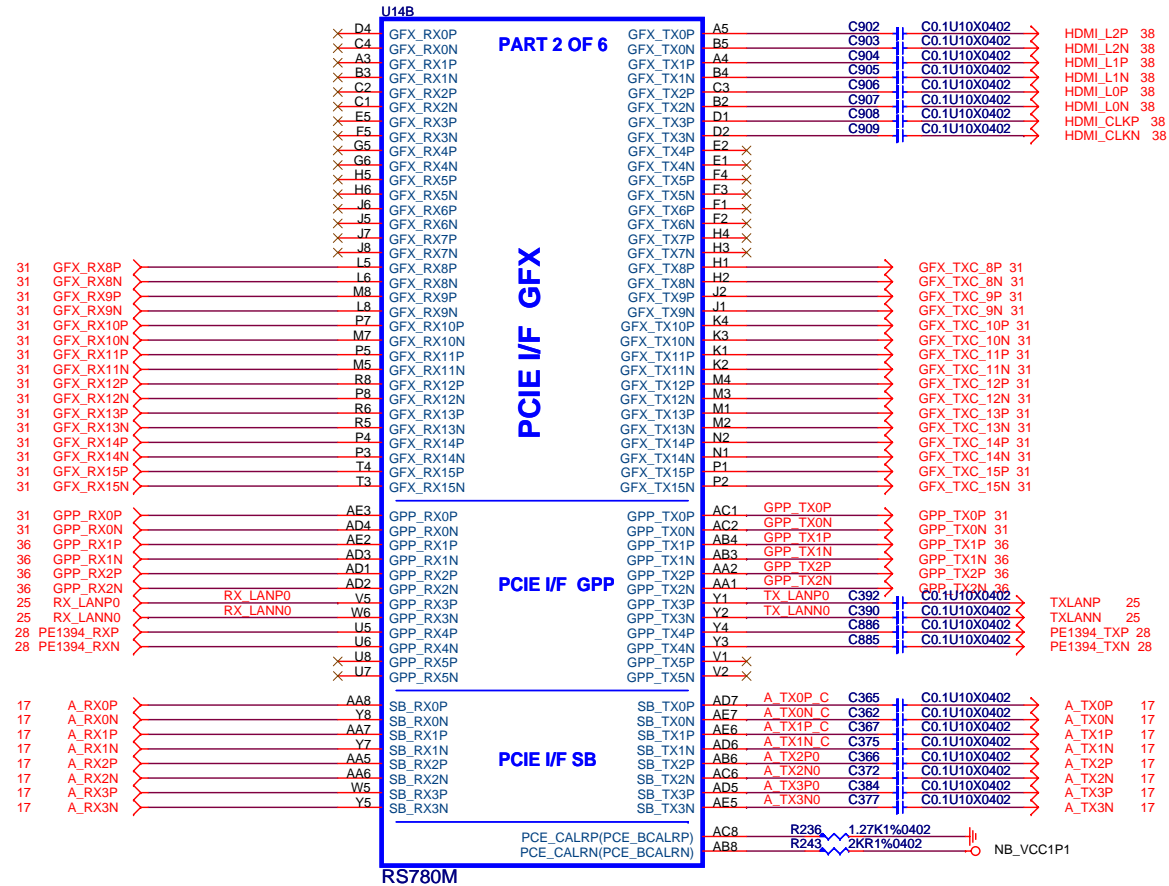


32MX16 DDR2 400 1.8V



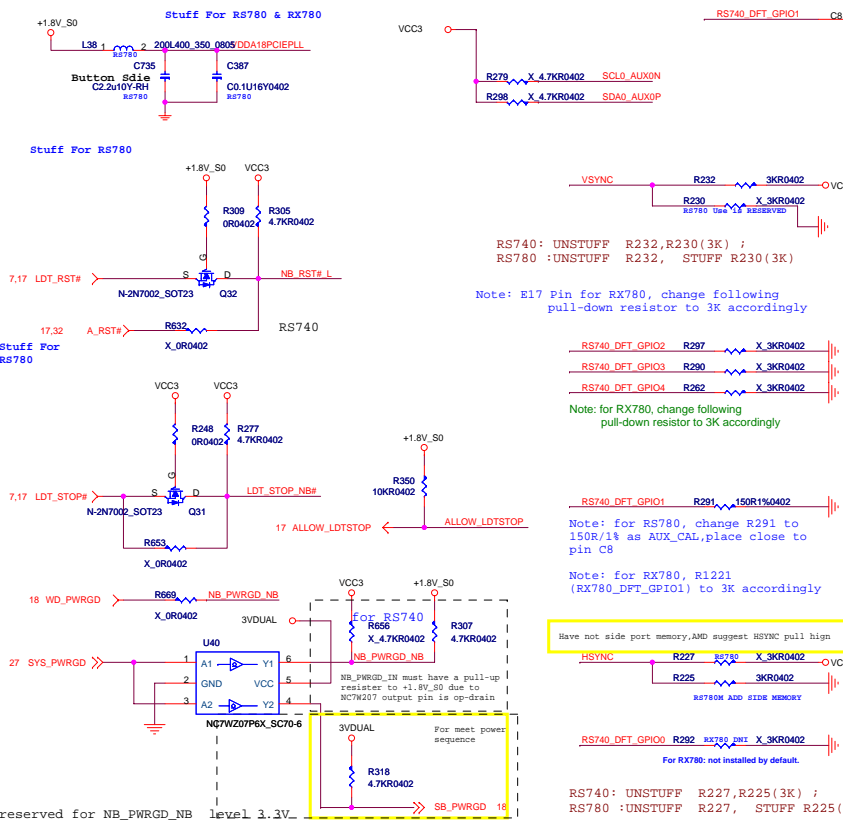
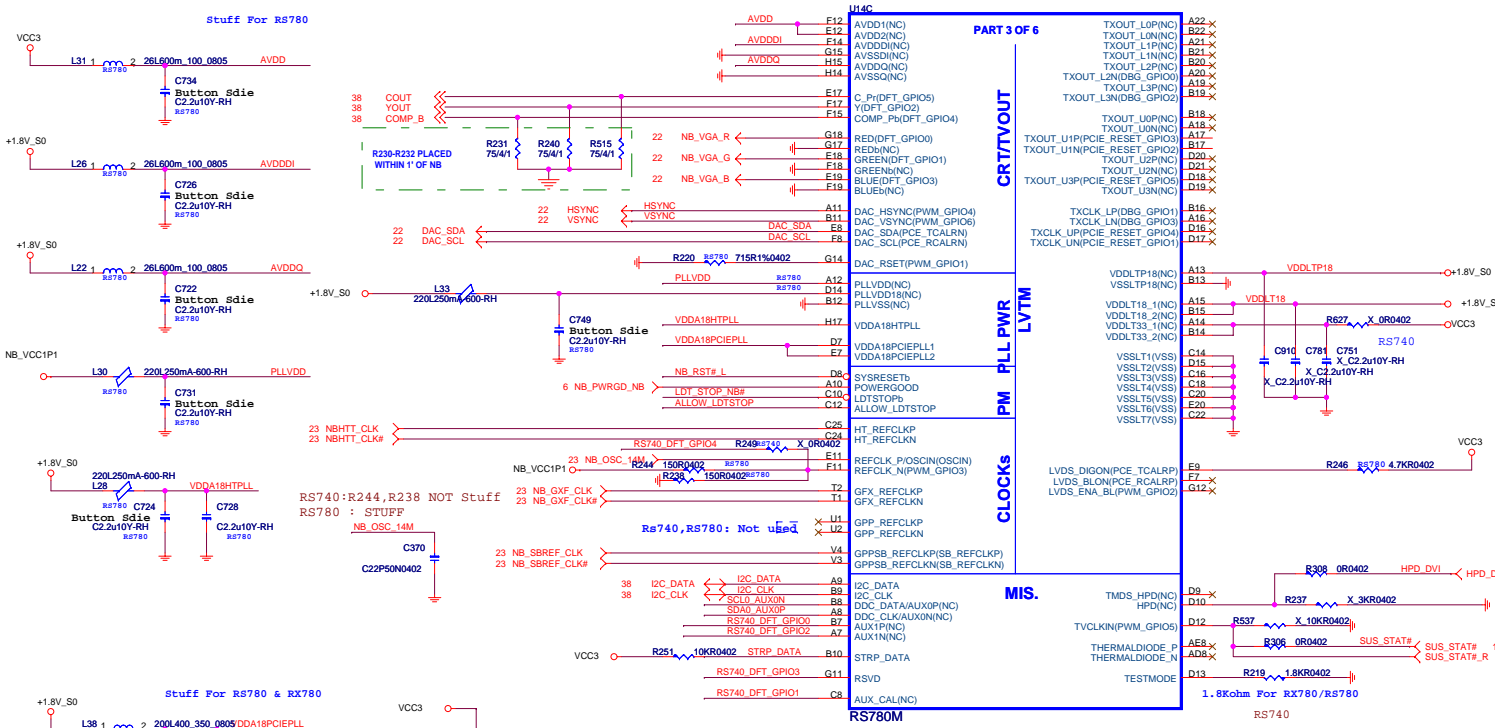


# RS780-PCIE I/F





# RS780-SYSTEM I/F



## RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLOK	LVDS_BLOK
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUXIN
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUXIP
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

### RS740/RX780/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO  
 1 : Disable (RS740); Enable (RX780/RS780)  
 0 : Enable (RS740); Disable (RX780/RS780)  
 RS740: pin DFT\_GPIO5  
 RX780: pin DFT\_GPIO5  
 RS780: pin VSYNC

### DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.  
 111: register defined (register default to Config E) default  
 110: 4-0-0-0-0 Config A  
 101: 4-0-0-0-0 Config B  
 100: 4-2-2-0-0 Config C  
 011: 4-2-1-1-0 Config D  
 010: 4-1-1-1-1 Config E  
 others: register defined (default to Config E)

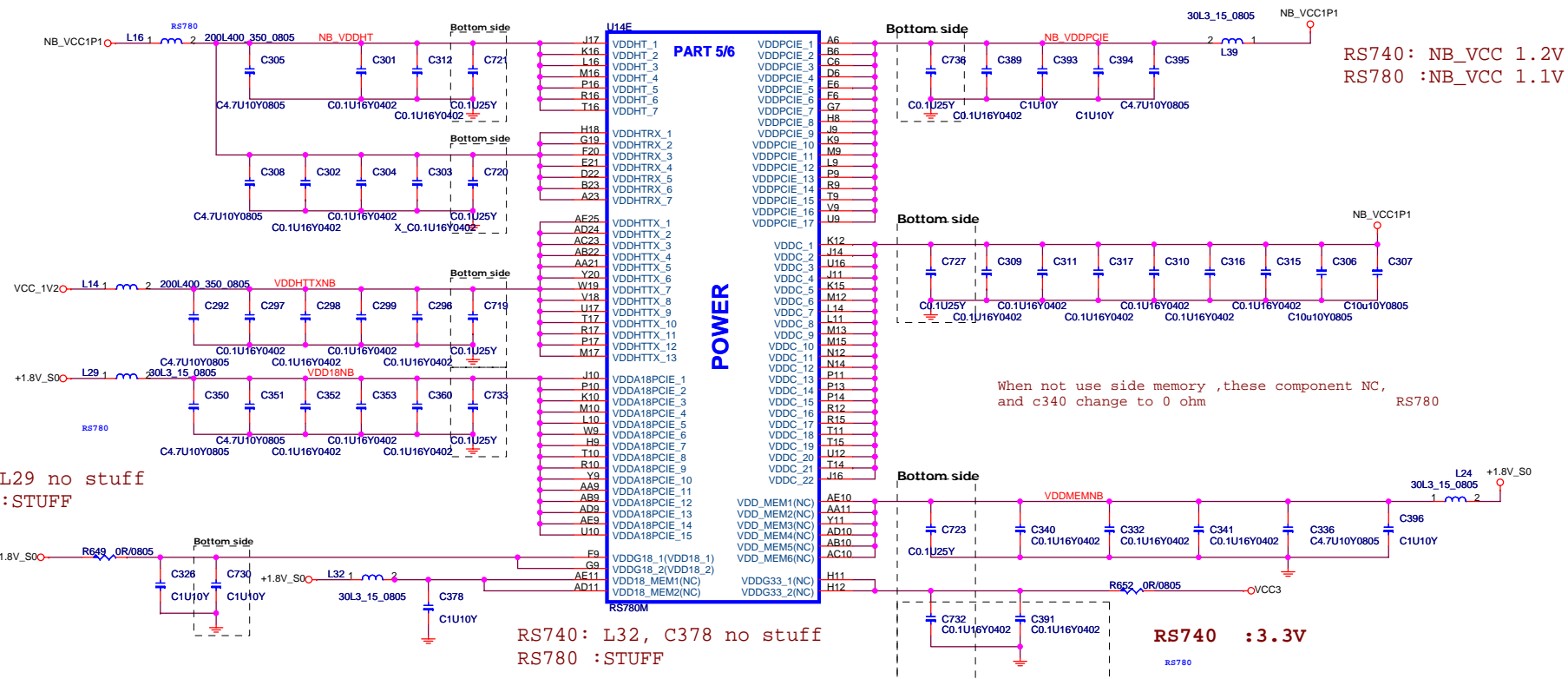
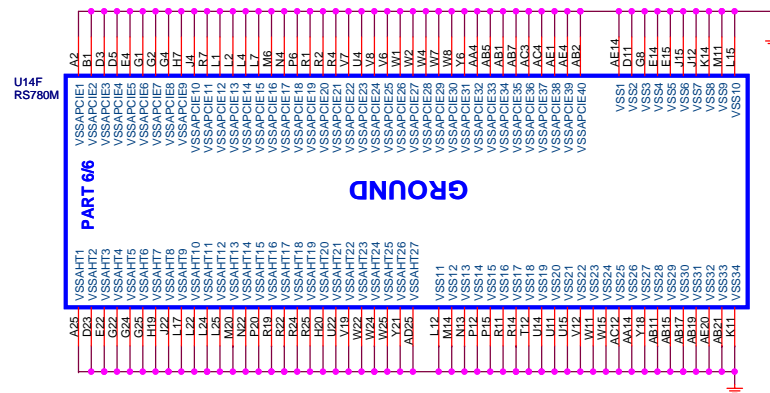
### RS740/RX780/RS780: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected  
 RS740: pin DFT\_GPIO1  
 RX780: pin DFT\_GPIO1  
 RS780: pin SUS\_STAT#

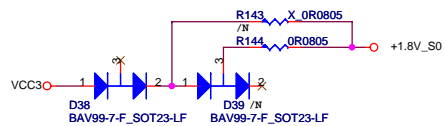
### RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory  
 1. Disable (RS740/RS780)  
 0 : Enable (RS740/RS780)  
 RS740: pin DFT\_GPIO0  
 RS780: pin HSYNC  
 RX780: Not Applicable

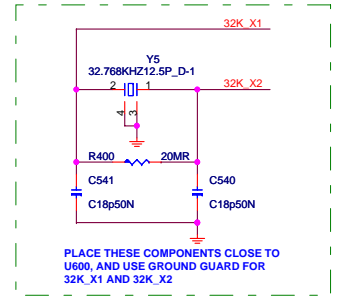
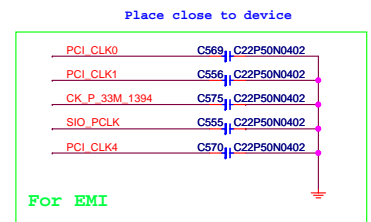
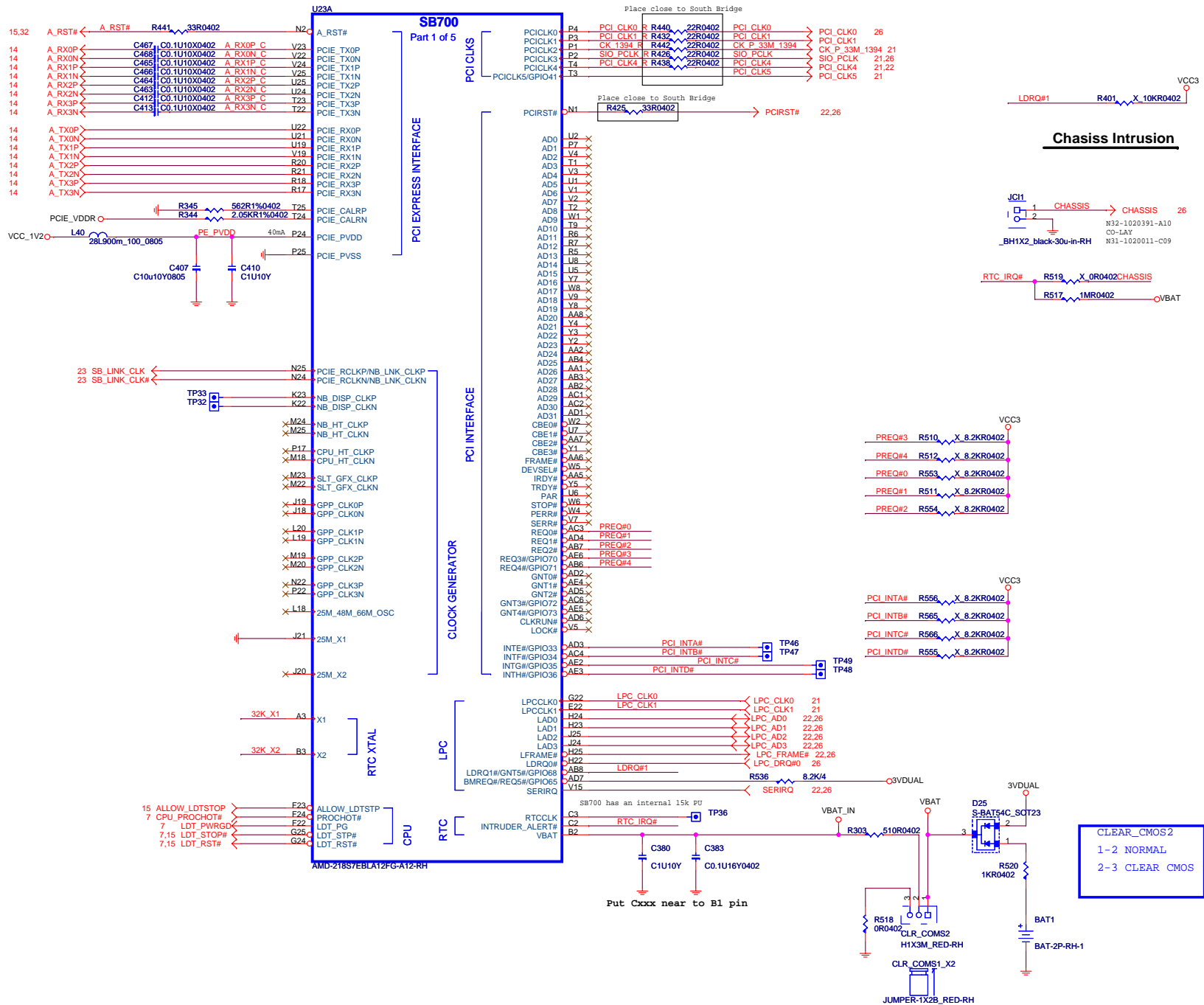




Resere RS690 North Bridge power sequence solution.

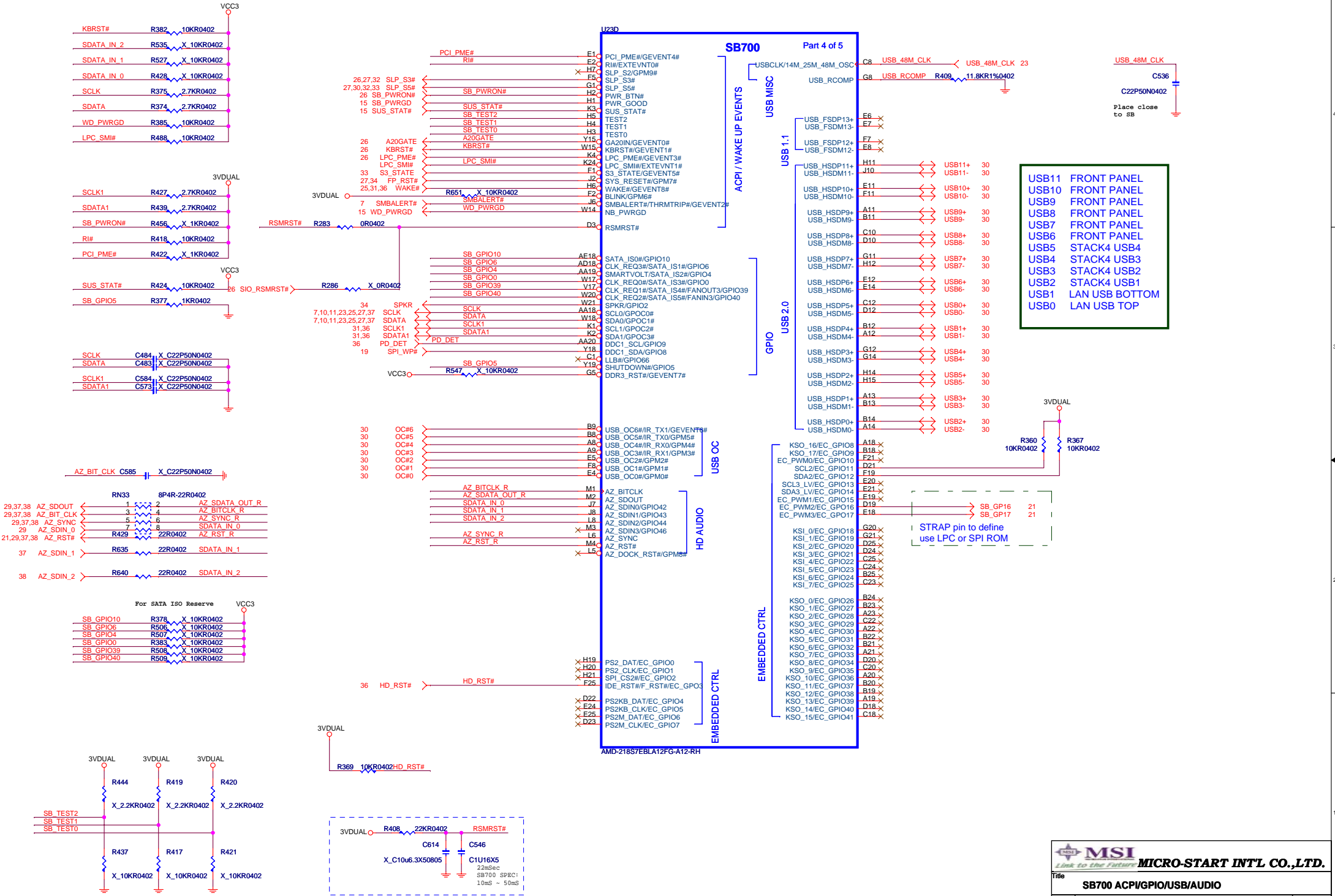




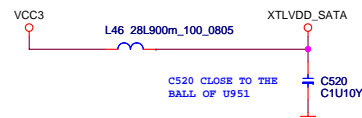
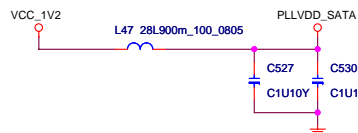
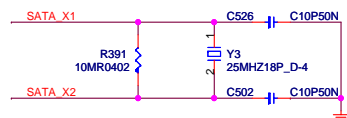
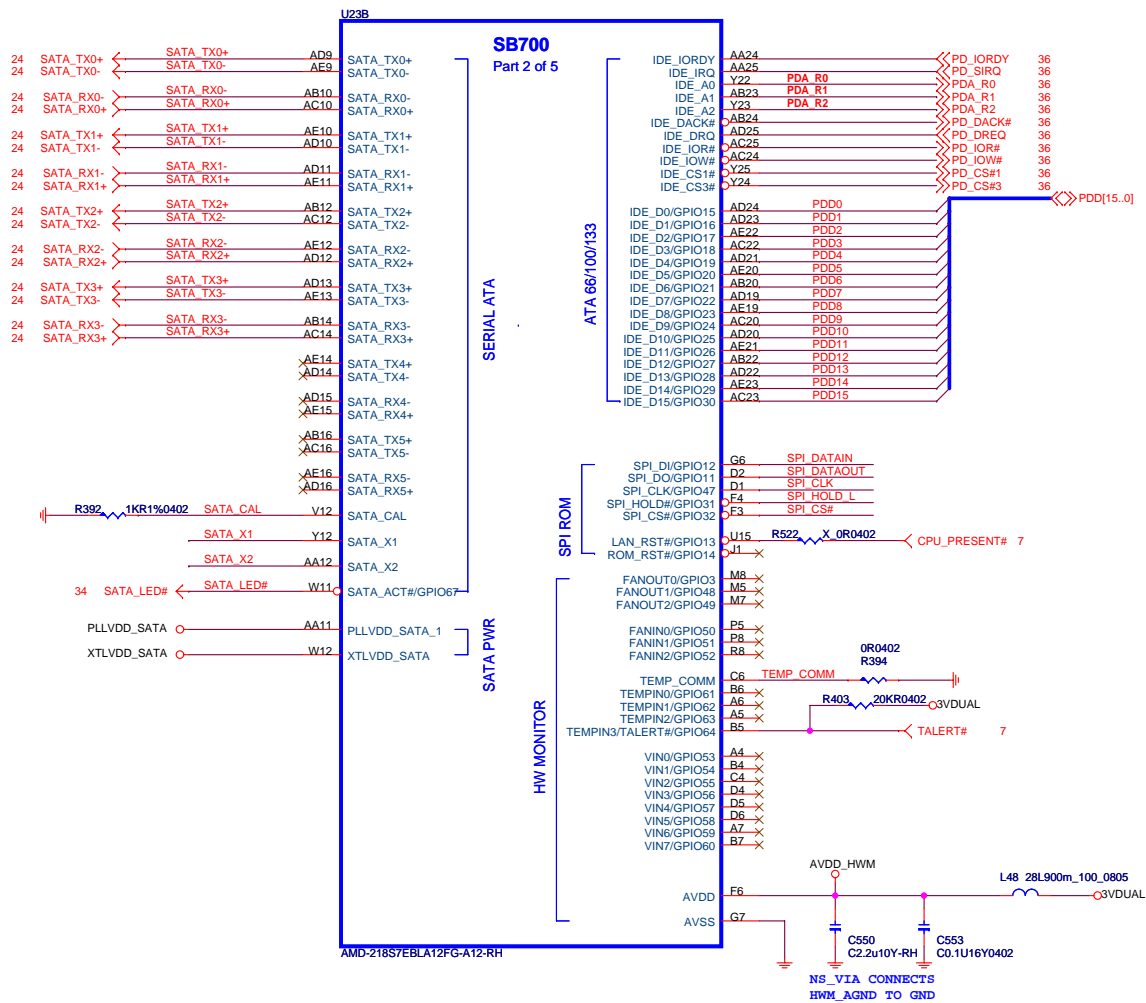


CLEAR\_CMOS2  
1-2 NORMAL  
2-3 CLEAR CMOS











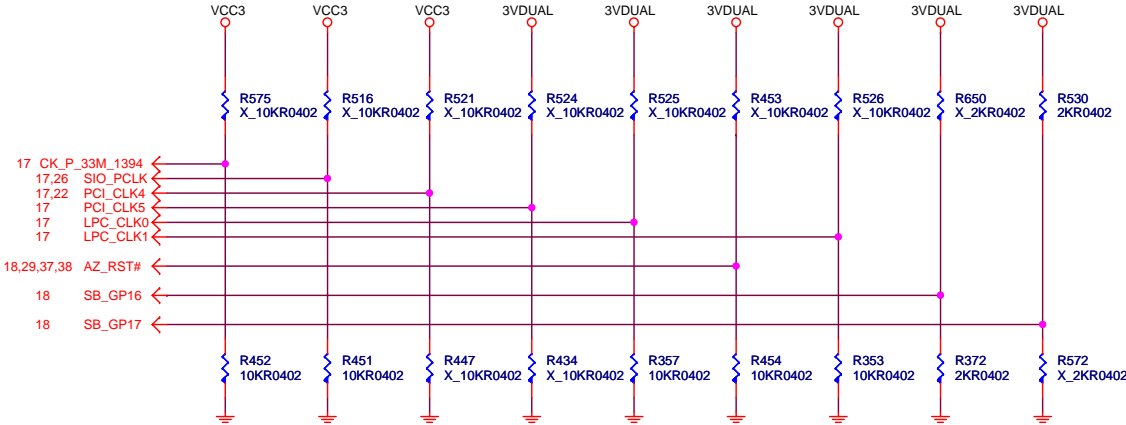






# REQUIRED STRAPS

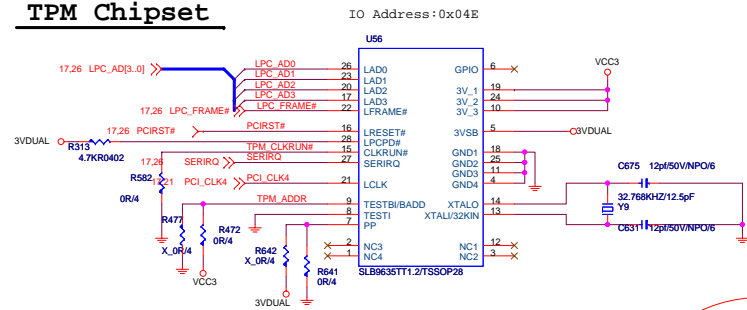
SB600 HAS 15K INTERNAL PD FOR AC\_SDATA\_OUT,  
15K PU FOR RTC\_CLK, EXTERNAL PU/PD IS  
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE  
REQUIRED



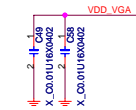
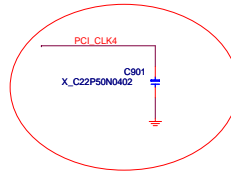
	PCI_CLK2 CK_P_33M_1394	PCI_CLK3 SIO_PCLK	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17   GP16	
	Watchdog timer on NB_PWGRD	Debug straps	TPM CLOCK	RESERVED	Booting from PCI Memory	Internal Clock Generator	INTERNAL RTC	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM <b>DEFAULT</b> L, H = LPC ROM L, L = FWH ROM	
PULL HIGH	ENABLED (VCC3)	ENABLED (VCC3)			ENABLED (VCC3_SB)	ENABLED (VCC3_SB)		ENABLED	Note: NC represents internal 10-k? 5% pull-up	
PULL LOW	DISABLED DEFAULT	DISABLED DEFAULT			DISABLED DEFAULT	DISABLED DEFAULT	NC IS EXT. RTC DEFAULT	DISABLED DEFAULT		



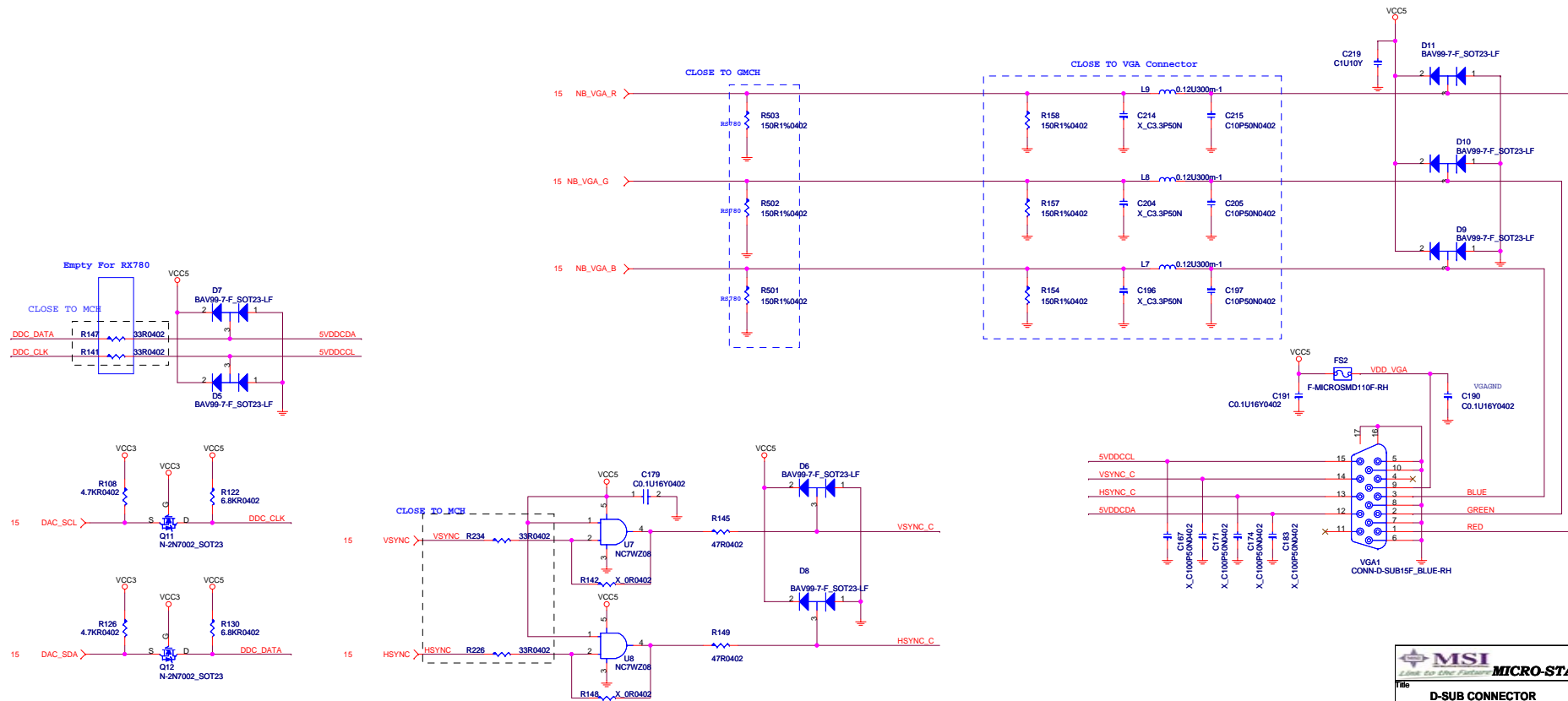
## TPM Chipset



PP : Physical presence  
standard connect to GND.

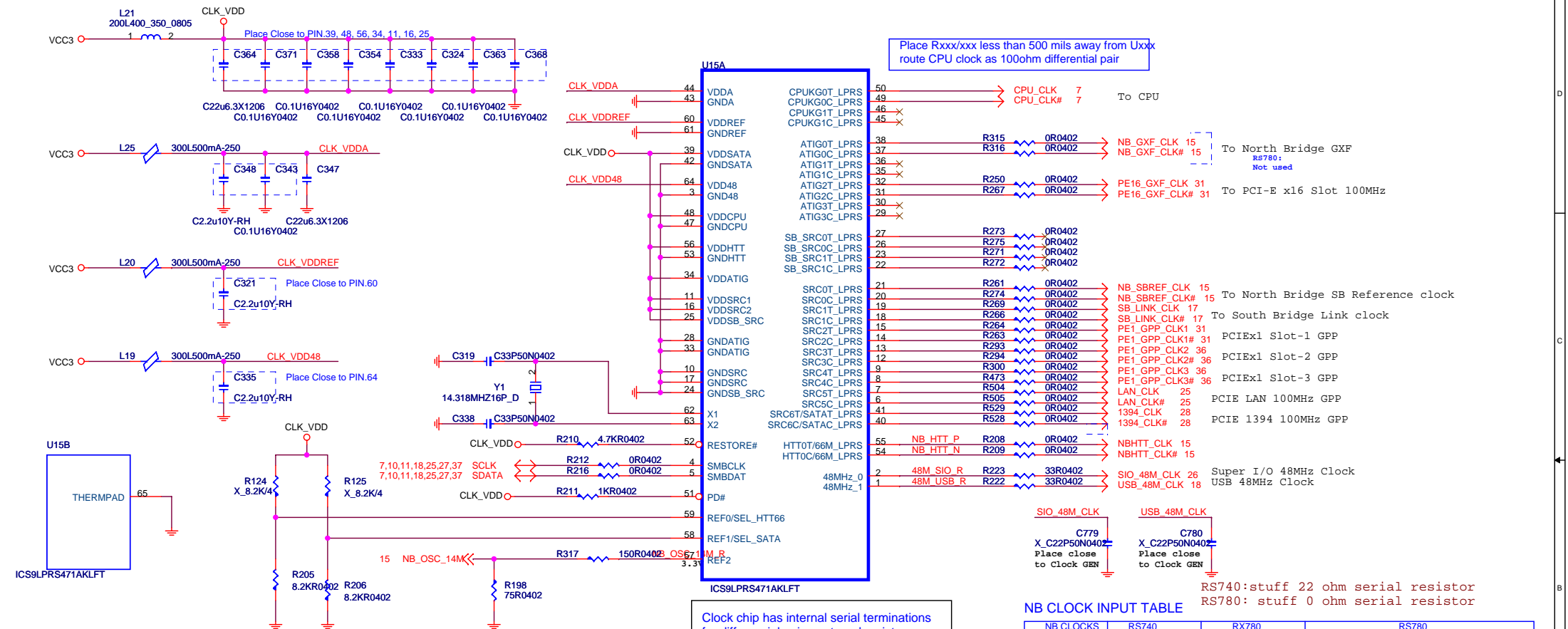


For EMI  
Placement close to ESD doide  
power pin.






Clock Gen ICS9LPRS471AKLFT



REF0/SEL_HTT66	HTT CLOCK	REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL	0	100.00 DIFFERENTIAL SPREADING SRC CLCOK
1	66.66 SINGLE END	1	100.00 NON-SPREADING DIFFERENTIAL SATA CLCOK

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPSSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

**MICRO-START INTL CO.,LTD.**

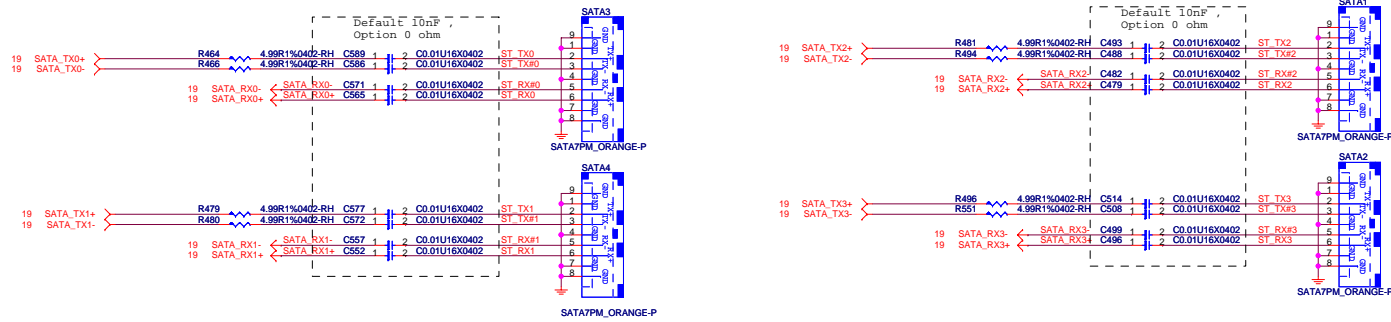
**Clock Gen ICS9LPR471**

Size	Document Number	Rev
B	<b>MS-7411</b>	<b>0B</b>

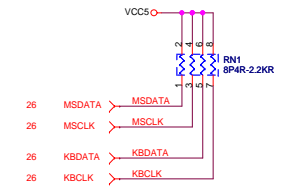
Date:	Wednesday, January 23, 2008	Sheet	23	of	39
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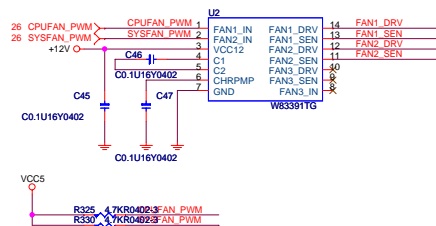
## SERIAL ATA CONNECTOR BLOCK



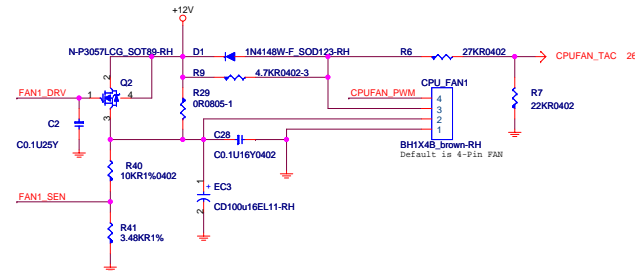
## PS2 KEYBOARD & MOUSE CONNECTOR



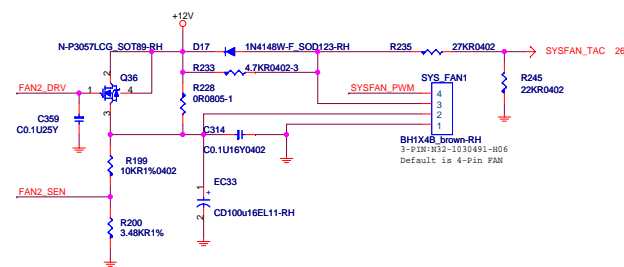
## PWM FAN CONTROL



## CPU FAN



### SYSTEM FAN









## 18F



## SUPER I/O STRAPPING RESISTOR

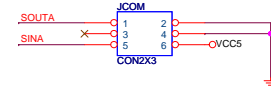


### Power On Strapping Options

Symbol	value	Description
Flashseg1_EN	1	Disabled.
	0	Flash I/F Address Segment 1 (FFFF_0000h-FFFF_FFFFh, 000F_0000h-000F_FFFFh) is enabled
VIDO_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
	0	Enable VIDOUT pins
CHIP_SEL	--	Chip selection in configuration.
BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
	0	The output buffers are push-pull.
FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
	0	The default value of EC Index 15h / 16h / 17h is 40h
VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
	0	The threshold voltage of VID is 0.8 / 0.4V

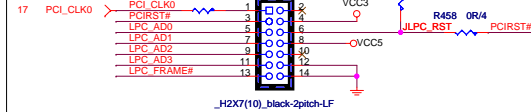
**BIOS WRITE PROTECT**

LED

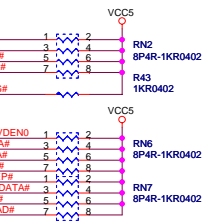


## SERIAL PORT 1

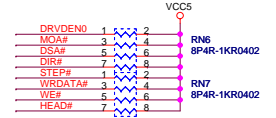
## LPC DEBUG PORT



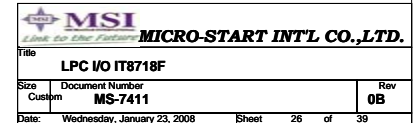
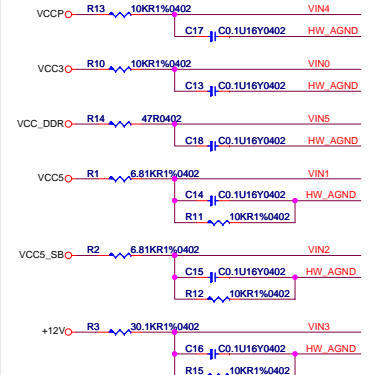
### Super I/O Chasiss



## FLOPPY CONNECTOR

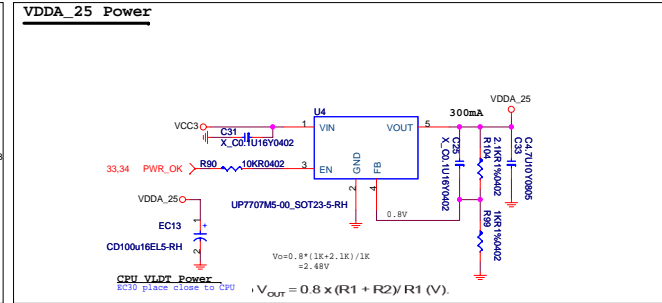
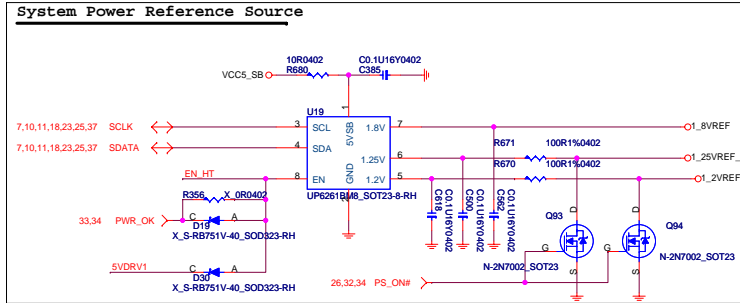
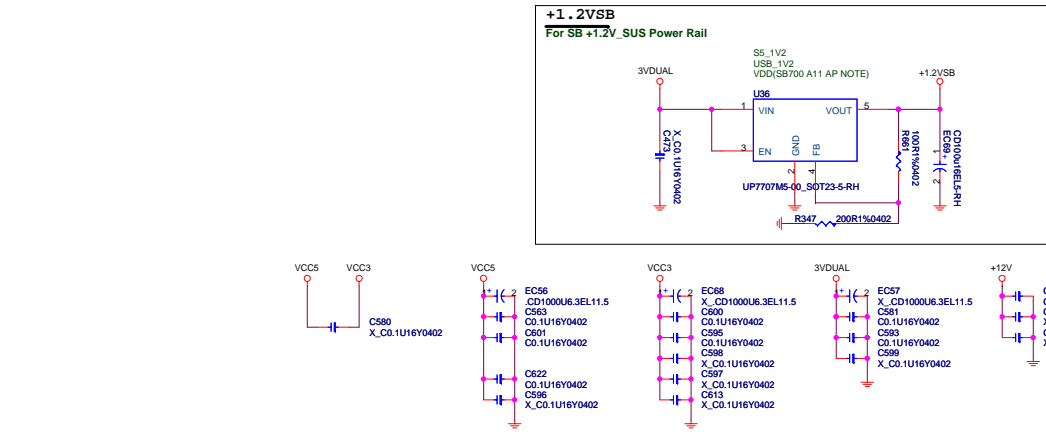
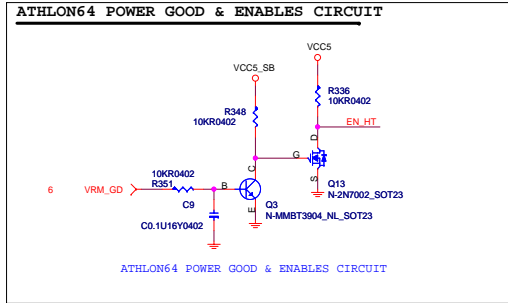


### Thermal Resistor



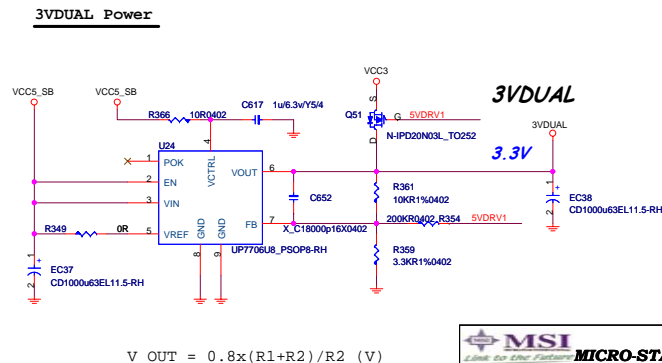
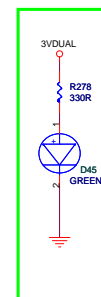
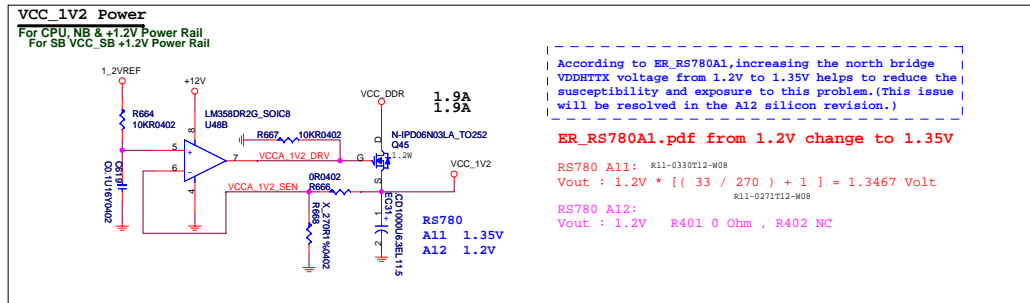


### SB700 & RS780 POWER GOOD CIRCUIT



Power Group A	Power Group B
VDDIO <sup>1,2</sup> Vcc_DDR	VDD[1:0] <sup>3</sup> Vcore
VTT <sup>1,2</sup> VTT	VDDNB        Vcore_NB
VDDA        VDPA25	VLDT        HT

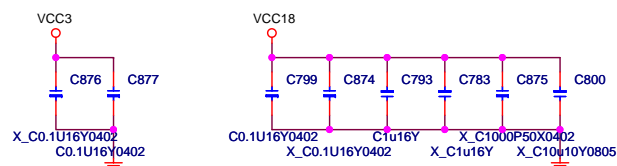
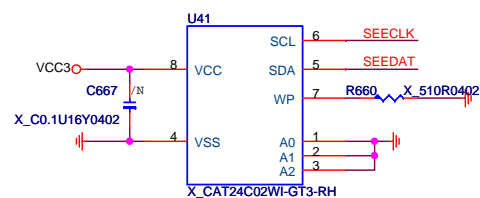
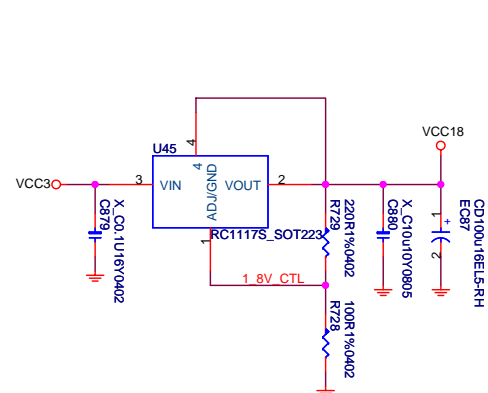
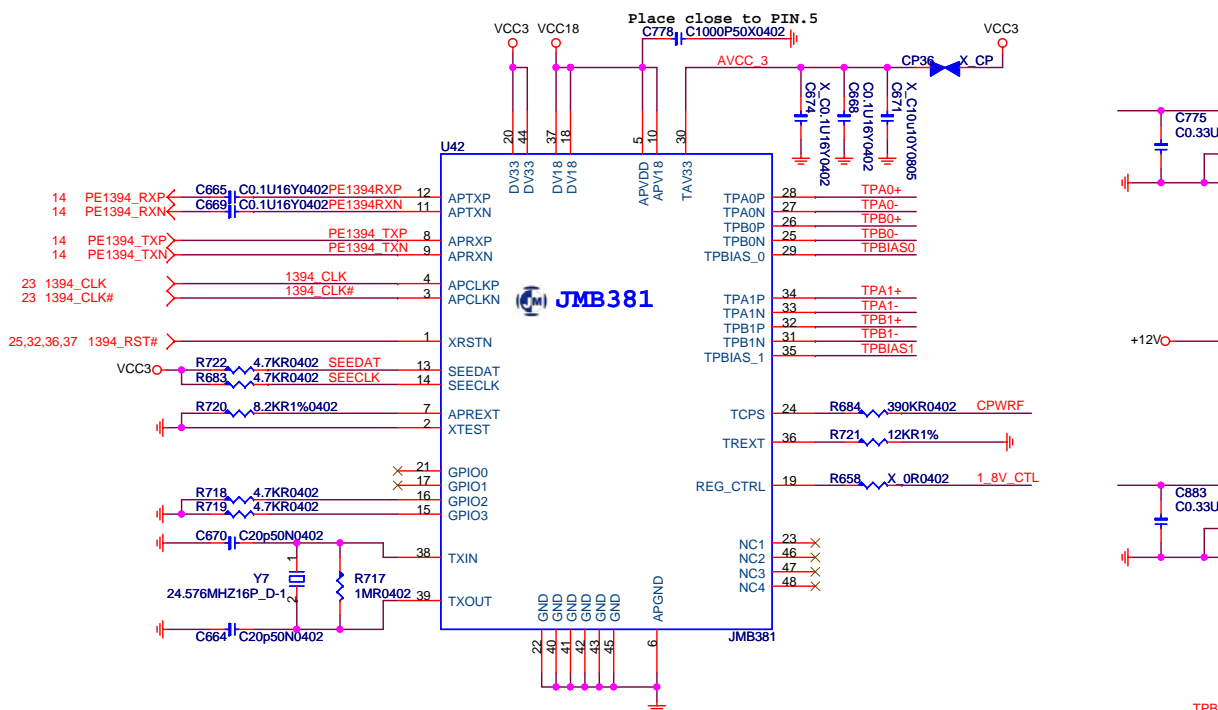
- 1) *VDDIO must never exceed VTT by greater than X.XX V. This relationship must be enforced at all times including power-up, power-down, and power failure.*
- 2) *VDDIO and VTT only apply to DDR2 compatible processors.*
- 3) *VDD refers generically to the core voltage plane(s). VDD0 refers to processor power plane 0, and VDD1 refers to processor power plane 1.*



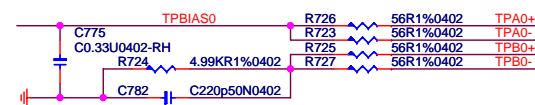
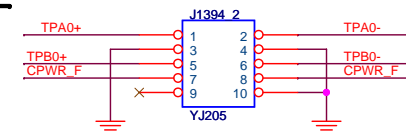
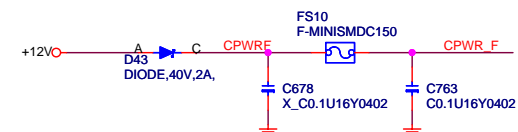
$$V_{OUT} = 0.8 \times (R1 + R2) / R2 \text{ (V)}$$



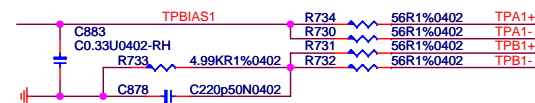
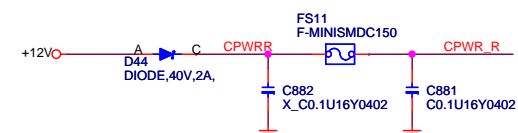
## IEEE 1394 - JMicron JMB381



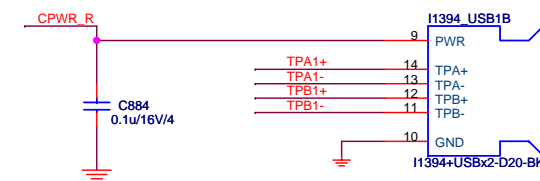
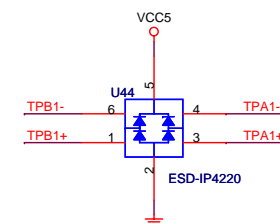
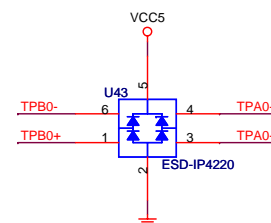
### Front Side IEEE-1394 Port



### Rear Side IEEE-1394 Port

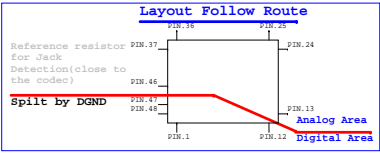


## IEEE-1394 Port ESD

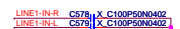




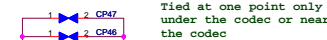
Default is ALC662



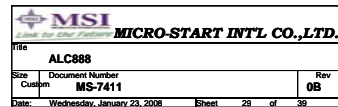
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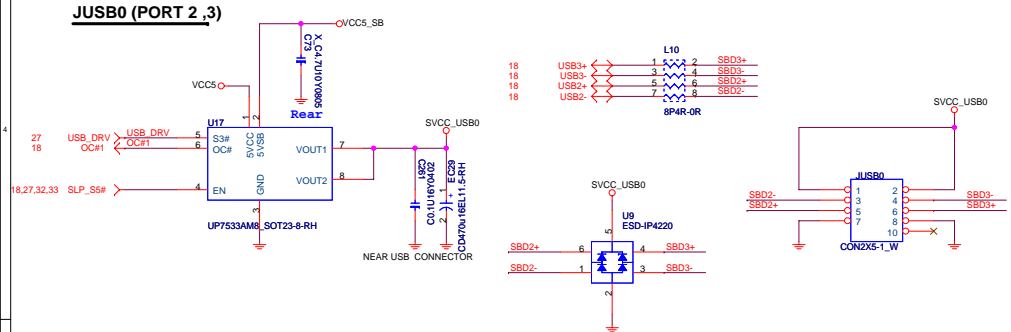


7 Tied at one point only  
8 under the codec or near  
the codec

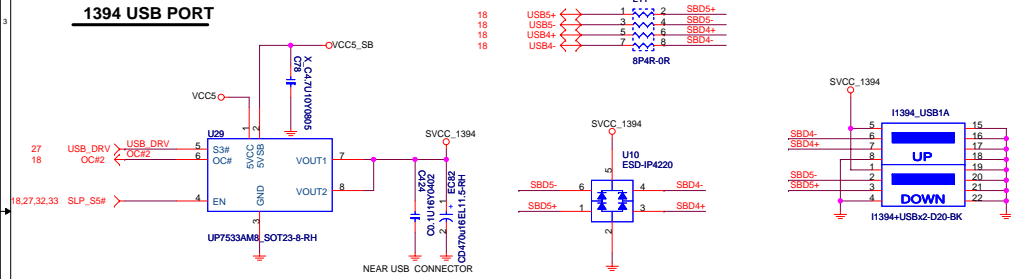




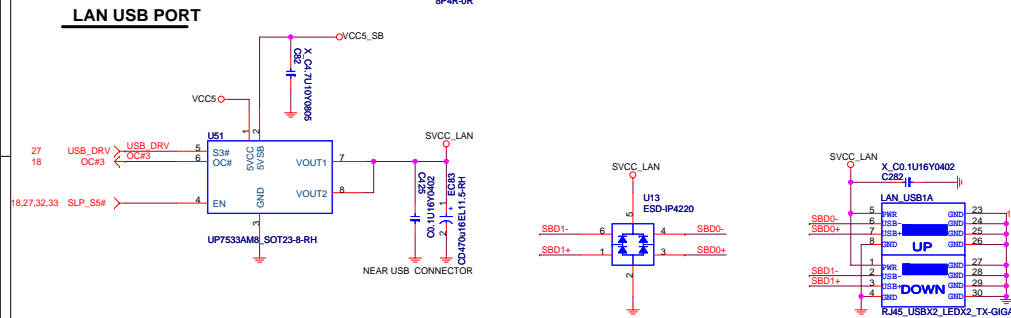
### JUSB0 (PORT 2,3)



### 1394 USB PORT



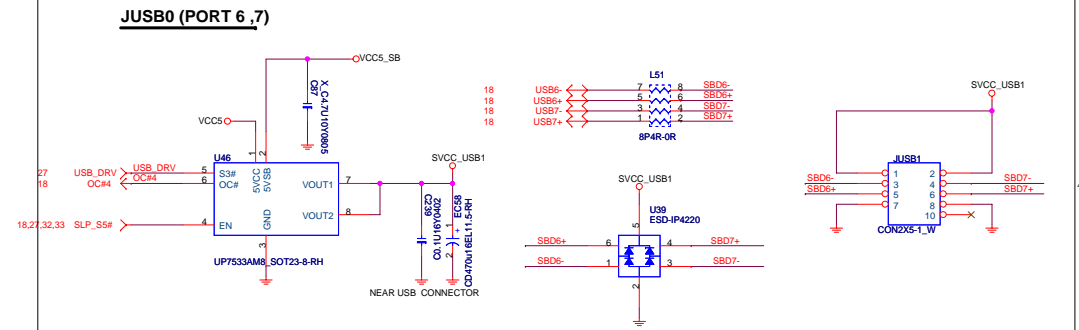
### LAN USB PORT



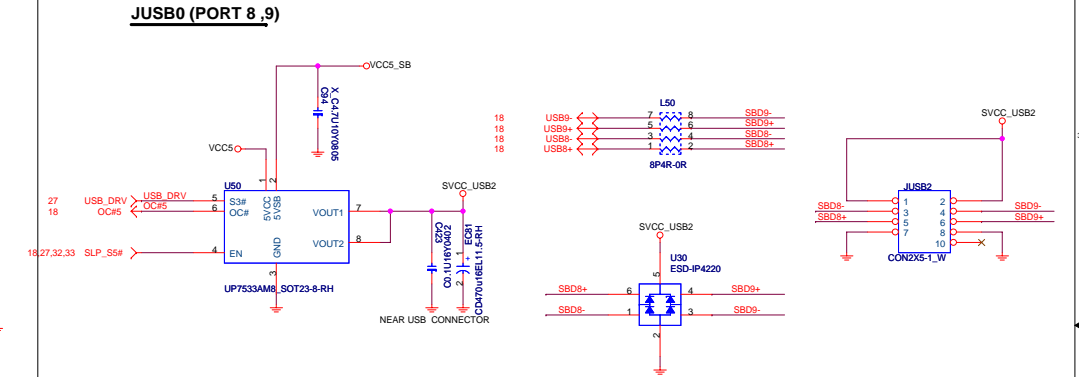
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

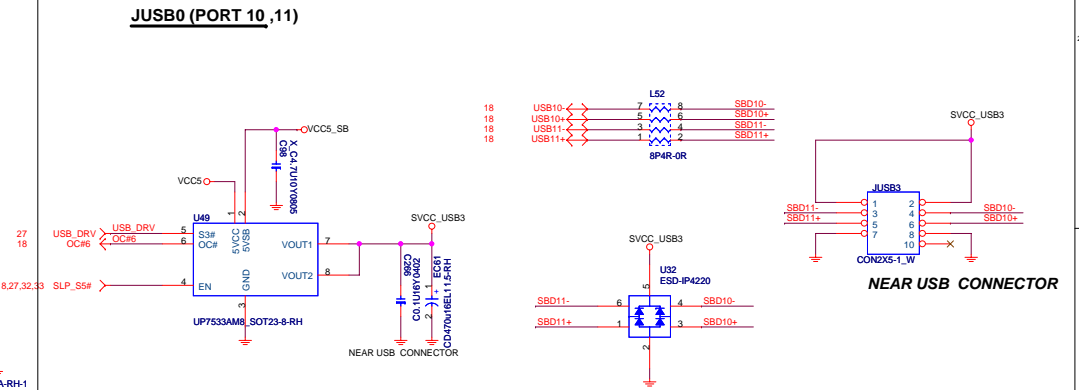
### JUSB0 (PORT 6,7)



### JUSB0 (PORT 8,9)



### JUSB0 (PORT 10,11)

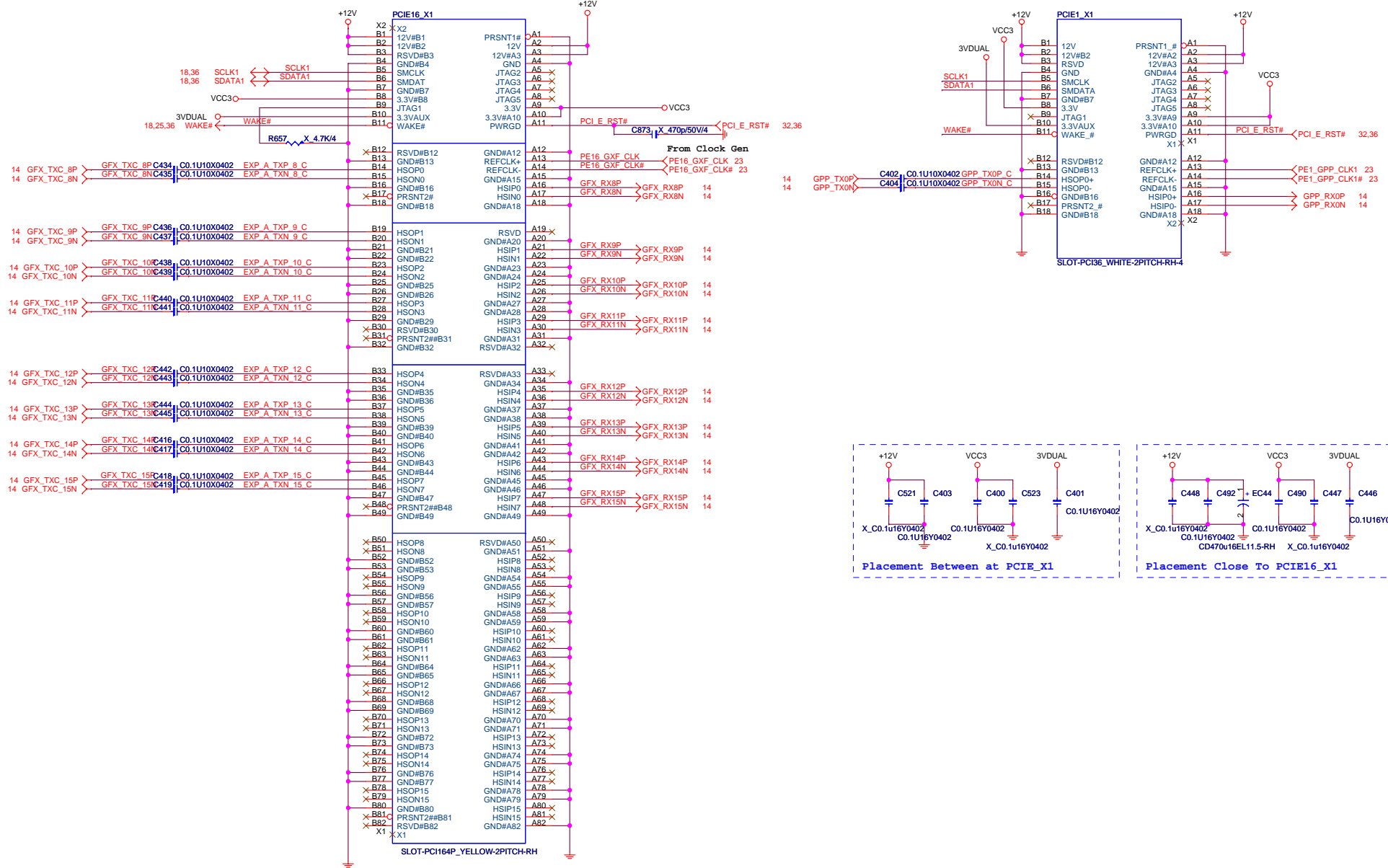




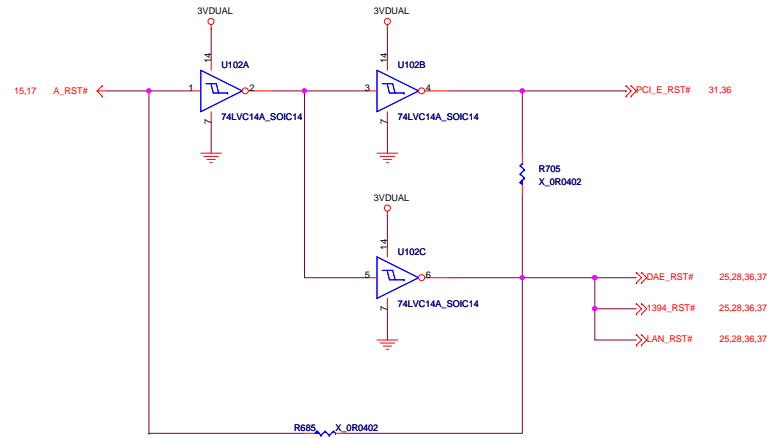
# PCI Express Slot x16/x1

## PCI EXPRESS x16 Slot

## PCI EXPRESS 1 Slot-1





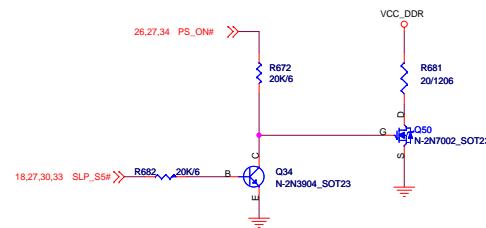
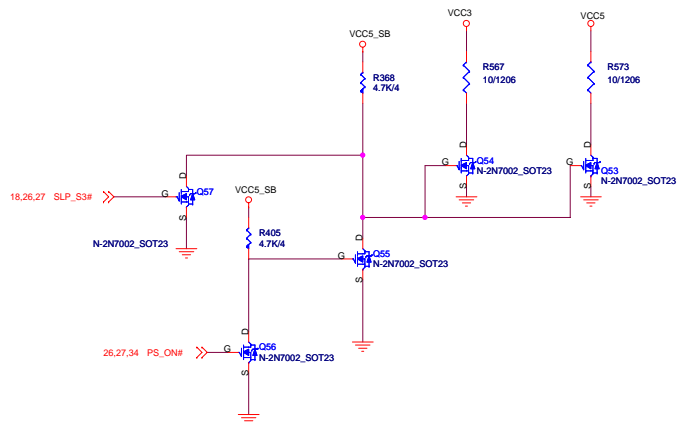


#### 7.1.6 Residual Voltage Bleed-Off Circuit

A residual voltage circuit is required on the board. This circuit must be active in the S3, S4, and S5 state, whenever the main +5 V and +3.3 V power are turned off. A circuit diagram is shown below. When the system is in S3, S4, or S5, the transistors will be turned on, which will clamp any residual voltage on +5V and +3.3 V to ground. See the figure below for an example of a bleed-off circuit.

#### MEMORY VOLTAGE BLEED-OFF CIRCUIT

#### BLEED-OFF CIRCUIT

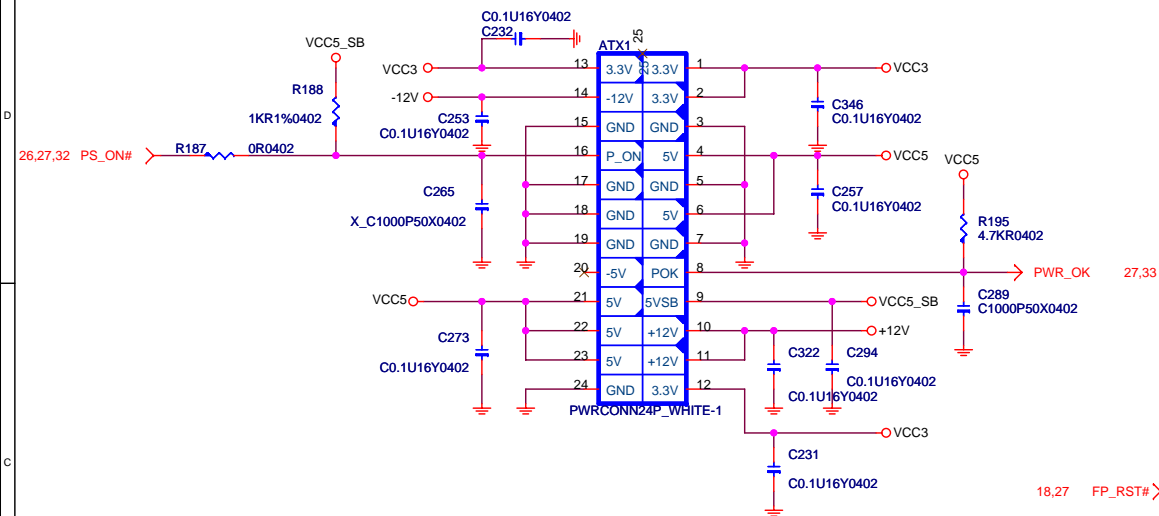




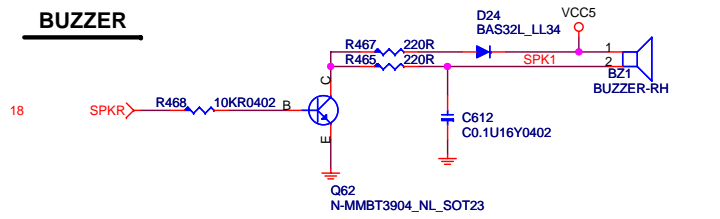




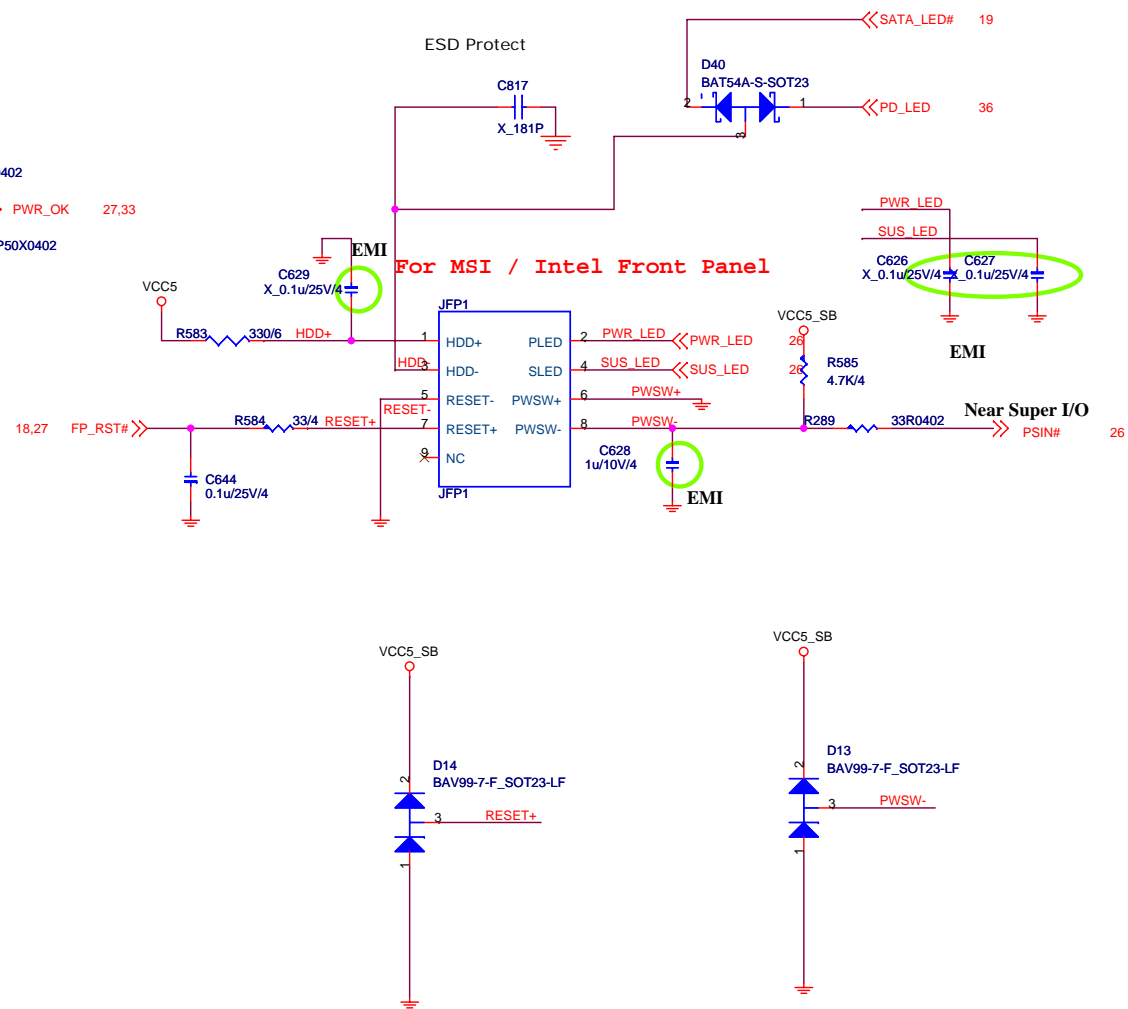
## ATX CONNECTOR



**BUZZER**

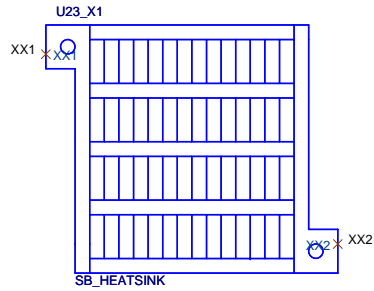
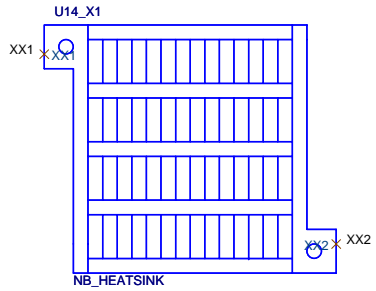


## Intel Front Panel

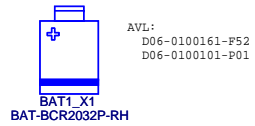




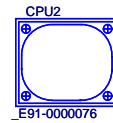
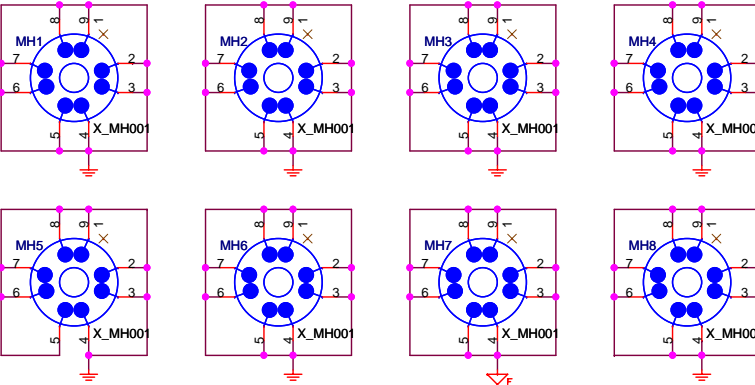
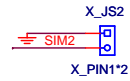
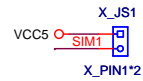
## HEAT SINK



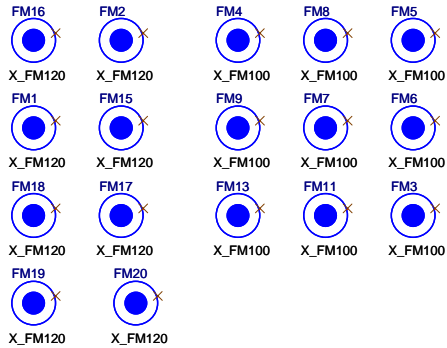
## MANUAL PART




## Simulation

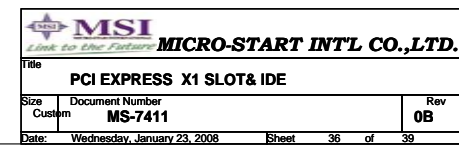
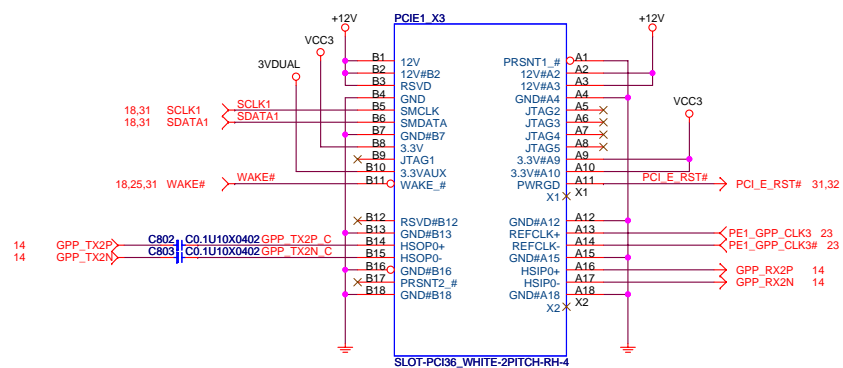


## Optics Orientation Holes

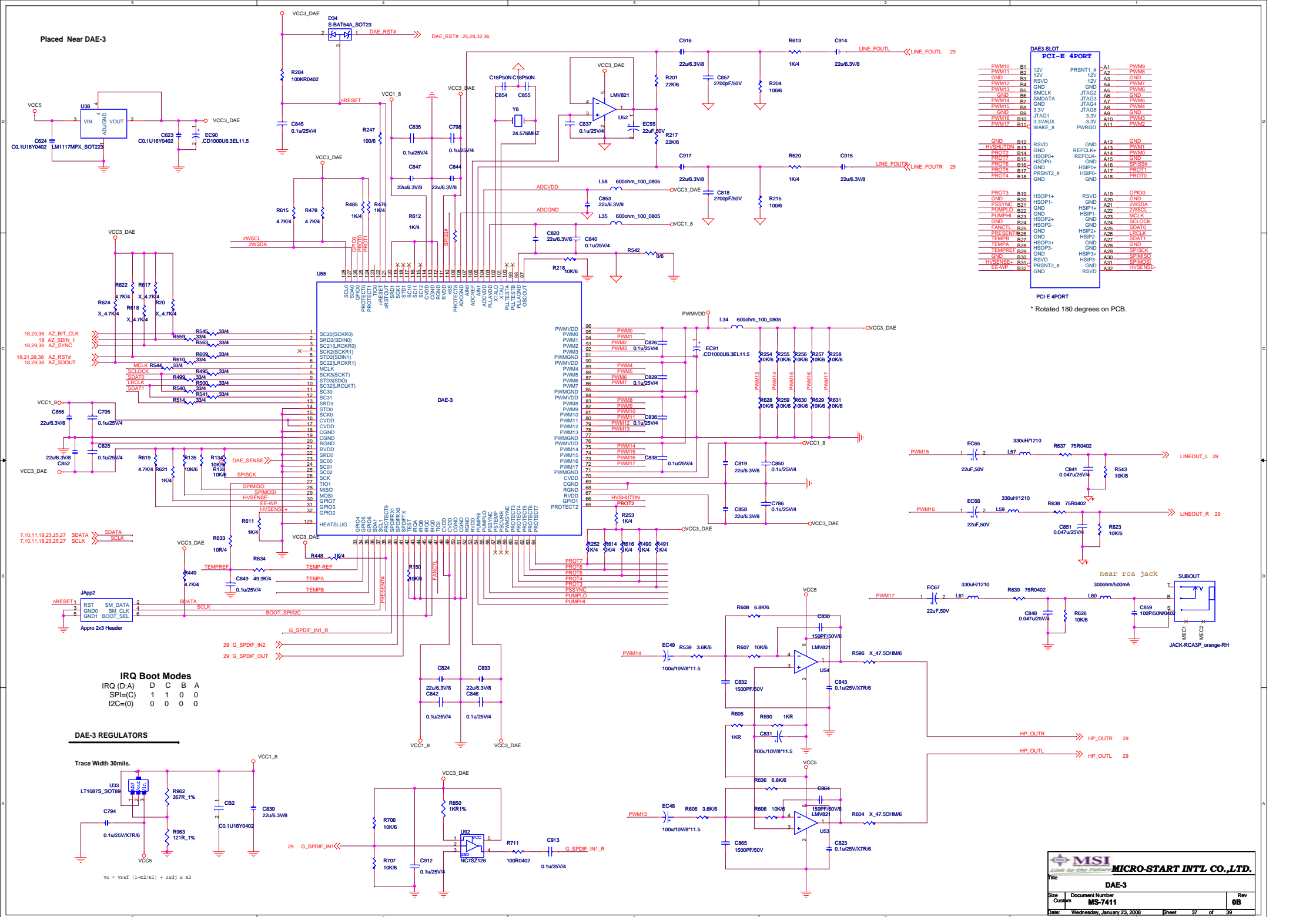


 <b>MICRO-START INTL CO.,LTD.</b>		
Title		
Auto BOM Mnaual		
Size B	Document Number	Rev
	MS-7411	0B
Date:	Wednesday, January 23, 2008	Sheet 35 of 39





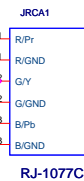
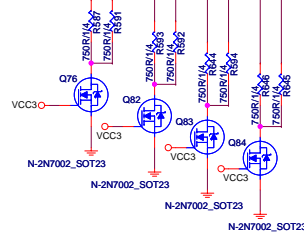
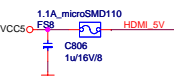






策臂,策稍

NOTE :reserve R188,R190,R193 2007/3/28



M6465 support VIDEO component out  
2007/3/24